Open-Loop Clock and Data Recovery Systems

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CDR circuits typically use PLLs, but their complexity presents several design challenges [1]: 1) the input data stream is random and is usually in non-return-to-zero (NRZ) data format, and little energy exists at the clock frequency that is to be recovered. Consequently, the choice of phase detector is very limited. Binary phase detectors are simpler in design but generate significant discontinuity on the control voltage of the VCO at each data transition edge. Linear phase detectors do not affect the VCO when they are phase-locked, but typically produce detection dead zone, which is due to short "UP" pulses, at high frequency applications; 2) The charge-pump current mismatch produces unequal "UP" and "DOWN" signal strengths, which causes the phase to drift from desired values; 3) The phase detector alone covers a very limited locking range, and frequency acquisition aids such as frequency detectors or switching between a training signal and real input data are usually required to increase the lock range; 4) A large capacitor is usually necessary in the LPF, which is not amenable to integration. If an off-chip capacitor is used instead, it requires an additional pin and increases cost.

In this paper, an open-loop CDR system based on injection-locking was adopted to avoid the aforementioned design challenges regarding PLL based CDR. It is known that when a signal with amplitude $V_{Injection}$ is injected into a free-running VCO, the VCO will injection-lock to the injected frequency as long as the difference between the VCO free running frequency and the injected signal frequency is within the lock range [2]:

$$f_{LOCK} = f_{OSC} \frac{V_{Injection}}{2 \cdot Q \cdot V_{oscillation}} \qquad (1),$$

where Q, V_{OSC} and f_{OSC} are the tank quality factor, the VCO oscillation amplitude, and the free-running oscillation frequency, respectively. The phase difference θ between the VCO output and the injection signal at the frequency f_{INJ} in injection-locked mode is given as:

$$\theta = \sin^{-1}\left(\frac{f_{OSC} - f_{INJ}}{f_{LOCK}} \right) \qquad (2).$$

No frequency or phase detector is necessary to maintain a constant phase relationship between the input and the recovered clock, which is a critical design constraint for data recovery circuits.

A block diagram of the injection-lock CDR is shown in Fig. 1 [3]. The input data stream is split into two branches: one for clock recovery and one for data recovery. Two 100Ω transmission lines terminated with 100Ω resistors are used at the input for power splitting and for 50Ω input termination. In the clock recovery branch, the harmonic generation block excites super-harmonics of the input data sequence to generate sufficient energy at the desired clock frequency to injection-lock the VCO. In the data recovery branch, limiting amplifiers (LA) are used as delay buffers, and also to maintain a constant input amplitude to the master/slave (M/S) latches. A dummy LA (DMY LA) is included to match the delays in the signal paths that feed to the voting logic. The delayed data is captured by M/S latches, compared using the majority voting logic, and then stored by another M/S latch. Another LA is used before the 50Ω output buffer to filter the clock glitch. Note that one objective of this paper is to investigate the effect of injection strength on the locking range. Consequently, the clock recovery circuit is not attached after the DMY LA, thus providing the flexibility of adjusting the injection signal strength to the VCO. Because LAs are used as the delay chain, the CDR also performs amplitude limiting to simplify the design of front-end amplifiers, which usually comprises of several LAs and/or an automatic gain control loop.

Details of the clock recovery branch and example timing waveforms are shown in Fig. 2 [4]. Since the phase information is only contained at data transition edges for the NRZ data format, the input binary stream is differentiated to perform edge detection and is then rectified. Rectification is a non-linear process, which generates super-harmonics from the input data stream that is used to injection-lock the VCO. The VCO is emitter degenerated to achieve a higher oscillation frequency and to provide a wider tuning range, while providing better phase noise performance [5][6]. The VCO outputs are separated: $V_{50\Omega+/-}$ are fed to 50Ω output buffers, while $V_{DR+/-+}$ are outputs of open-collector buffers to drive the data recovery circuit.

The half circuit of the M/S latch and the majority voting logic are depicted in Fig. 3, where the clock signal is locally terminated by a resistor at each latch input. The delay of the voting logic is only one NAND gate delay, compared to two NAND delays in the implementation in [3]. It can be observed that exploiting different output node voltages of the latches simplifies the voting logic and also minimizes the delay, such that voting can be completed in one clock cycle. In [3], the voting result is not latched, which may result from the longer delay of the voting logic. An example operation of the voting logic is explained in Fig. 3, where the inputs “A” and “B” to the voting logic have the same data value, and therefore the output mimics “A” and “B”. The nominal delay of the delay chain was designed such that when f_{OSC} is close to f_{INJ}, “B” aligns to the centre between data transition edges to reduce the BER. From (2) it can be observed that variations of this delay against PVT can be mitigated by increasing $V_{Injection}$. A simple calibration circuit can also be included to adjust the VCO control voltage if necessary. As long as the locking range is wide enough, which can be achieved by generating large $V_{Injection}$ through the proposed super harmonic generation technique, the exact delay of the delay chain and the exact VCO control voltage is not critical for the proposed injection-locked CDR.

The CDR is fabricated using 45-GHz f_T IBM SiGe BiCMOS 6HP technology. However, the same concepts can be implemented in CMOS. A 10 Gb/s, 400mVpp differential PRBS of length 2^7-1 is fed to the CDR inputs. The output spectrum in free running and injection-locked mode for the same VCO control voltage is shown in Fig. 4. When injection-locked, the VCO frequency shifts from the free running frequency to the injection signal frequency without the use of frequency or phase detectors. Example eye diagrams in locked and out-of-lock modes are shown in Fig. 5. According to the 1.77ps input data RMS jitter (when the oscilloscope is triggered by a precision signal source) and the 2.21ps recovered data RMS jitter (when the oscilloscope is triggered by the recovered clock), the incremental jitter caused by the CDR is less than 1.32ps. The BER as the function of VCO control voltage is shown in Fig. 6. The fabricated CDR achieves injection-locking with a BER lower than 1e-12 over a 160-MHz free-running VCO frequency range. The design is pad-limited where the active area is 730µm x 680µm as shown in the die photo in Fig. 7. At 3.3V the clock recovery circuit, the data recovery circuit and the output buffer stages consume 35mW, 195mW and 175mW, respectively. Lastly, the proposed CDR can scale with technology leading to more energy efficient implementation.

References

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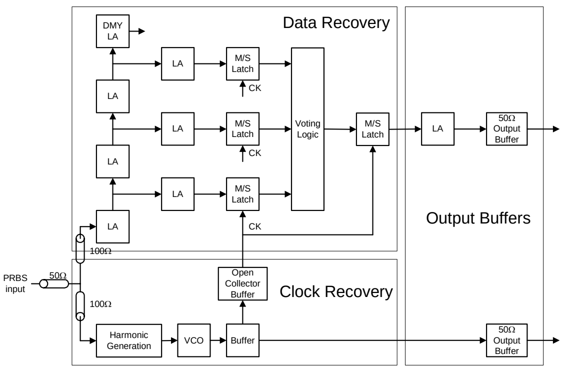

Figure 1: Block Diagram

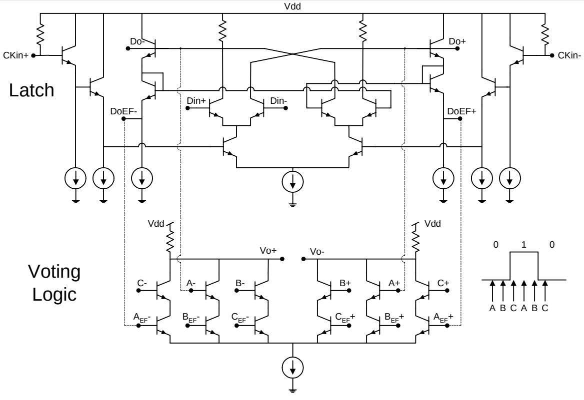

Figure 3: Schematic of latch and voting logic

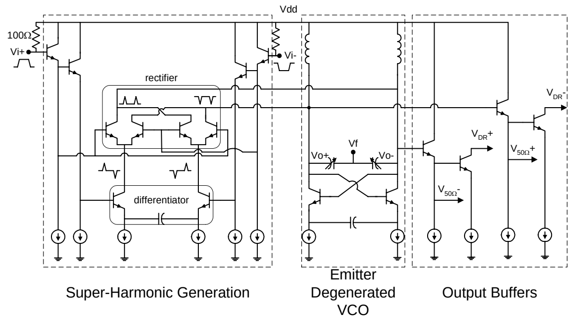

Figure 2: Schematic of clock recovery circuit

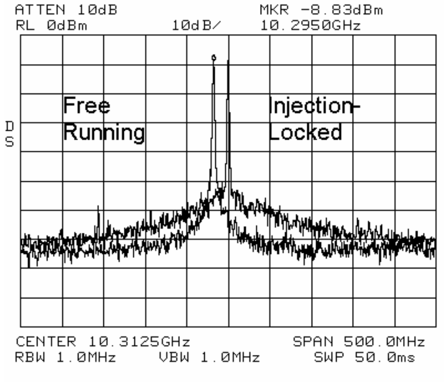

Figure 4: Example spectrum in lock and free running modes

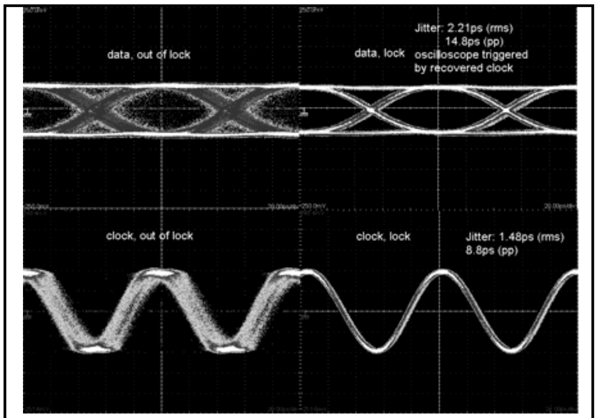

Figure 5 Recovered clock and data

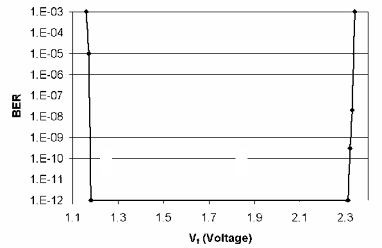

Figure 6: Bit error rate as a function of VCO control voltage

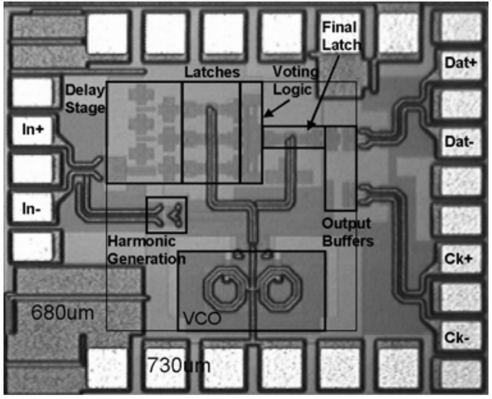

Figure 7: Chip microphoto