

Modeling and Extraction of Interconnect Parasitic under Process Variation

PI: Weiping Shi
Department of Electrical Engineering
Texas A&M University
College Station, Texas 77843

IBM Technical Contact: Frank Liu
IBM Austin Research Lab
Austin, Texas 78758

1. Motivation:

An important link is missing in the current methodology for timing verification of VLSI circuits: the link between the parasitics extracted from layout and the actual parasitics of the fabricated circuits. As sub-wavelength lithography is extended with OPC/PSM, the geometry of the fabricated interconnect looks increasingly different from the perfect geometry in the designed layout. In addition, the shapes of the conformal dielectrics are very hard to specify and rarely considered by the existing parasitic extraction algorithms. As a result, the extracted parasitics could be off from the actual parasitics by a large margin. It directly affects the validity of static, dynamic and statistical timing verification. A similar link is missing in the current research on statistical timing analysis: the link between the assumed process variation models and the real process variation models, for interconnect parasitics. As a result, current statistical timing verification has to assume a conservative and pessimistic model. As the interconnect delay becomes more dominant and the needs for statistical timing verification increase, it is an urgent task to build realistic yet simple interconnect parasitics models under process variation. This project will establish the missing links, by providing the community with 1) statistical models of interconnect parasitics under process variation, and 2) a manufacturing-aware extraction methodology that computes interconnect parasitics using mathematical methods and test chips. Successful completion of this project will increase the chance that fabricated chips meet the timing requirements, increase the functional yield and parametric yield.

2. PI Previous Related Research:

For parasitic extraction, we proposed a 3D capacitance extraction algorithm that is significantly faster than previous 3D algorithms and received a Best Paper Award from DAC 98. We also proposed a solenoidal basis algorithm for 3D inductance extraction that is much faster than FastHenry. A number of techniques were developed to improve the speed and accuracy of 3D capacitance extraction, including a divide-and-conquer algorithm and variations of BEMs. Recently, we invented a novel preconditioning

technique to for solving capacitance extraction problems, and even completely eliminated the iterative solver.

For timing verification under process variation, we proposed a method to simplify the statistical model of process variation using Singular value Decomposition (SVD), without sacrificing the accuracy. We also developed parametric static timing analysis under process variation, for finding longest paths for delay test, and an efficient method to compute parametric delay as a function of process variables. We have developed the only tool that can find the longest sensitizable paths and applied it to a large industrial design. We will use this in path-based statistical STA.

3. Research Plan:

Existing 2D/2.5D LPE methods are based on formulas or pre-characterized libraries, which are computed by 3D field solvers. Both the interconnect layout and the libraries assume perfect geometry.

We will compute the formulas and libraries using a modified geometry. The modified geometry gives the same parasitic as the actual fabricated geometry, but is much easier for 3D field solver to compute. This way, the existing LPE methods can be used, except with the new extraction formulas and libraries. We will study how to modify the perfect geometry to simulate the fabricated geometry. This can be done through litho/etching simulation. Our preliminary study indicates that with a few modifications to the perfect geometry, we can reduce the error of LPE to less than 1%. To compute the modified geometry, we will use litho/etching models and process parameters measured from test chips. In addition, we will develop 3D field solvers that can work with litho/etching simulation tools, where the distortions of the shapes are taken into consideration at the time of surface discretization.

Realistic models of interconnect parasitic under process variation are crucial for meaningful timing verification. Existing models are based on metal width, metal thickness and inter-layer dielectric thickness. However, little is know about the distributions of these process variations from the fabrication community. Using collected data, we will build statistical models of interconnect parasitic under process variation. Since the number of process variables is large, simplification is necessary. Techniques such as Principal Component Analysis and Singular Value Decomposition will be used to make the statistical models simple yet accurate. Special effort will be made to model correlated process variation.