

VLSI DESIGN, DESIGN AUTOMATION, VERIFICATION TECHNOLOGY AND PACKAGING

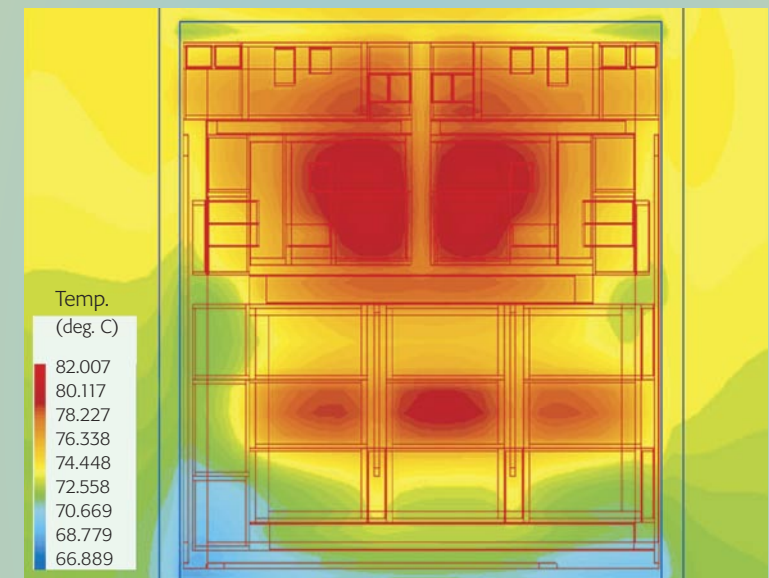
One of the striking aspects in the advancement of computer technology has been the continuing improvement in system throughput, increasing two-fold every 12 to 18 months. The continuing shrinking of devices and the concomitant increase in performance, following Moore's Law and Dennard scaling rules for device miniaturization, has played an important part in this progress. An equally important aspect, however, has been the continuing progress in VLSI circuit and chip design, design automation, design verification, and the packaging from chip to system level. IBM Research has been playing a key role in each of these areas.

VLSI DESIGN

Research has a long history of involvement with IBM high-performance processor design: from the pioneering 801 RISC processor of the 1980s and ground-breaking work in Very Long Instruction Word (VLW) architecture and systems to the first IBM mainframe with a CMOS microprocessor in 1996 and the current ultra-complex systems such as those using POWER5™. As the latest processor for IBM's iSeries™ and pSeries® systems, POWER5 uses eight levels of copper wiring and over a quarter billion transistors to take full advantage of IBM's leading-edge 130 nm. Silicon-on-Insulator (SOI) technology. Research continues to make major contributions to IBM's microprocessors, spanning the full spectrum of system design, including microarchitectures, circuits and circuit techniques, low power, design methodologies and tools, design verification, and interaction with technology development. A strong focus centers on developing advanced high-end systems. Along with industry collaborators, for example, Research is working with IBM's Systems and Technology Group in the development of future server processors, as well as the Cell Broadband Engine™ – the next generation of scalable and power-efficient microprocessors, a multi-core architecture optimized for computer-intensive rich media applications. IBM places a significant emphasis on System-on-a-Chip (SoC) design capabilities, in which pre-design components are used to quickly compose chips with high levels of function. Research contributes to IBM's SoC capabilities in both the design and tools areas. These capabilities played an integral part in the design of Blue Gene/L that became the world's fastest supercomputer in 2004.

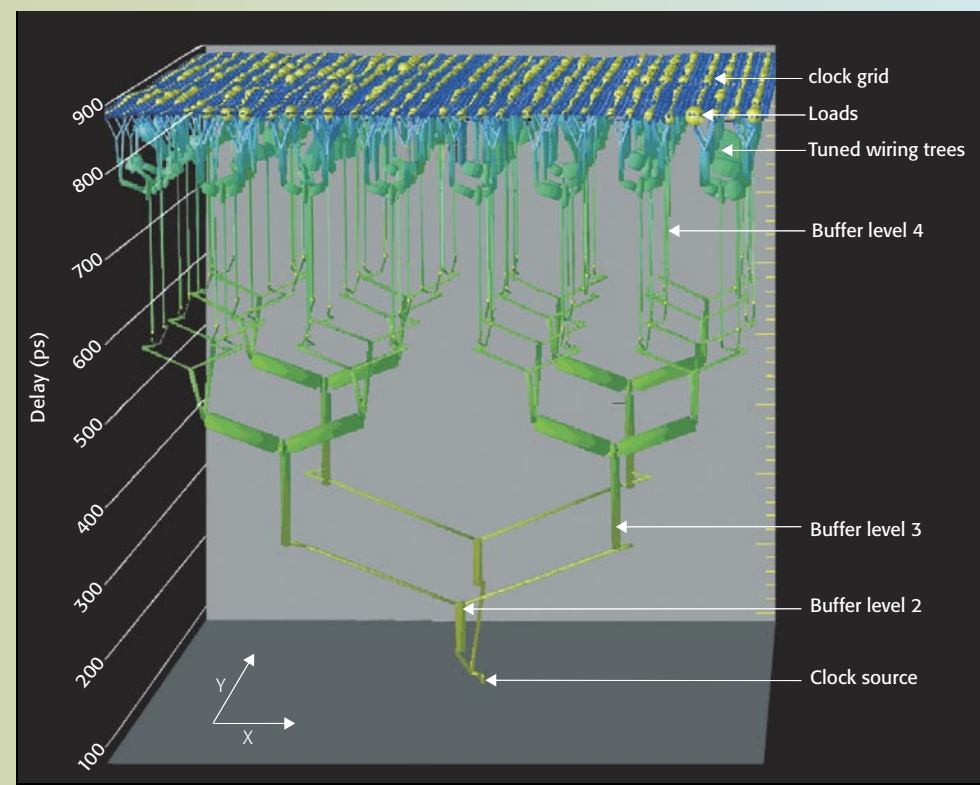
DESIGN AUTOMATION

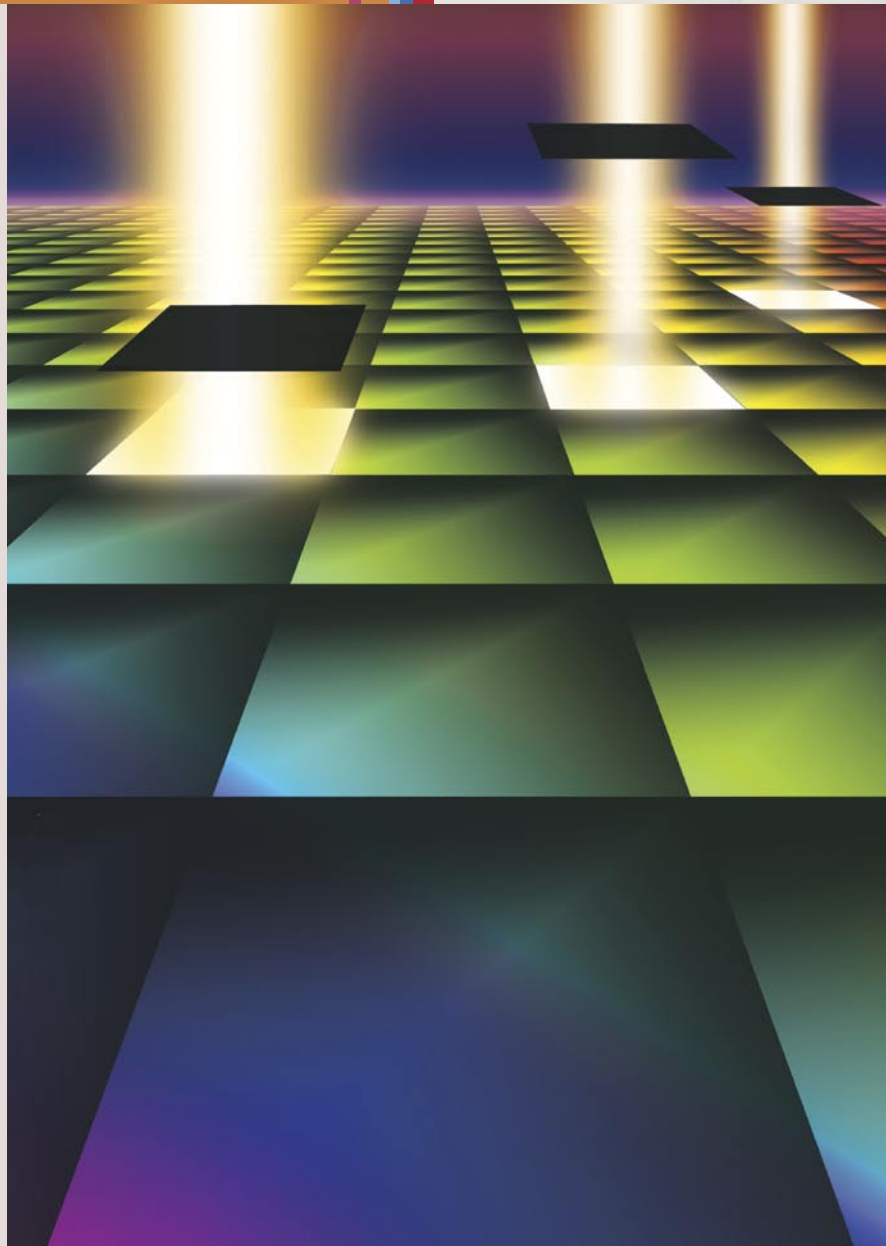
IBM Research has three decades of leadership in the development of world-class Design Automation (DA) tools for high-performance microprocessors and leading-edge Application-Specific Integrated Circuits (ASICs). It has pioneered the production use of logic synthesis, circuit tuning, design migration, and microprocessor power analysis. IBM's DA research relies on a close relationship with IBM's technology and design organizations to bring about unique Computer-Aided-Design (CAD) solutions, crucial to the success of IBM's microprocessor and ASIC designs. VLSI designers face many challenges: the widening designer productivity gap, the slowdown in CMOS scaling, the increasing complexity of system designs, the power density crisis, and the rising importance of statistical design techniques, due to increased complexity and variability in semiconductor manufacturing. The result is an unprecedented opportunity for design automation to provide integrated solutions and tools at every level of the design hierarchy and abstraction. Current DA projects focus on system-level design, logic and physical synthesis, interconnect modeling and analysis, statistical timing, design for manufacturing, and leakage power analysis and optimization.



Variation of temperature on a chip.

The clock distribution of the POWER4™ microprocessor.





Advanced test-program generation technology.

VERIFICATION TECHNOLOGY

Design verification centers on ensuring that the description of chip functionality written in a hardware description language like VHDL actually complies with the specifications of the chip and system operation. This is key to avoiding design errors and systems bugs and reducing time-to-market. IBM has been at the forefront of the research and development of functional verification for decades in both simulation-based verification technologies and formal verification.

The Property Specification Language (PSL), currently the subject of standardization by the IEEE, originated from the Research-developed Sugar language. IBM Research also pioneered the use of formal model-checking of industrial-strength designs with its RuleBase PE (Parallel Edition) verification tool, which has had parallelism recently incorporated to significantly enhance performance. Current research in formal verification is focused on using innovative algorithms to extend the size of designs that can be verified. Design verification techniques show promise for a wider variety of applications; for example, the applicability of formal model-checking to other domains, such as software systems, control systems, and business processes, is being explored.

Research specializes in the three major aspects of simulation-based verification: test-program and stimuli generation, functional coverage, and checking. Our test generation techniques, tools, and solutions, which focus on the verification of processors and large systems, are widely recognized as the best in the field. These technologies are being used extensively throughout IBM in all major hardware development labs. In coverage, IBM researchers were among the pioneers of using functional coverage in design verification. In this context, coverage analysis tools and a family of test generators were developed that specialize in specific design areas, and promote a verification approach based upon a systematic coverage-driven generation philosophy. To complete this technology, researchers are involved in

a project for Coverage-Directed Generation (CDG), which uses machine-learning techniques to automate the process of using feedback from coverage analysis for tuning generation stimuli towards areas not adequately verified. Another research direction is hybrid (semi-formal) verification, where the goal is to add formal verification capabilities to normal dynamic verification environments

ELECTRICAL INTERCONNECT AND PACKAGING

Research activities in electrical interconnect and packaging provide best-of-breed packaging, electrical designs, modeling/simulation tools, and characterization techniques for current and future server and supercomputer packaging needs, including cables, board, cards, multi-chip modules, single chip carriers, and on-chip interconnections. IBM invented C4 solder ball array packaging, led in thick and thin film packaging, and developed the Thermal Conduction Module (TCM) for its high-end systems. To model these advanced structures, Research built on its pioneering work of the 1970s in efficient numerical techniques for calculating the electromagnetic behavior of realistic package and chip structures to create an extensive suite of extremely powerful and accurate solvers, capable of modeling the largest problem size in the industry. ElectroMagnetic Surface modeling (EMSurf) and ElectroMagnetic Simulation (EMSIM) are full-wave, three-dimensional frequency domain solvers that can handle up to one million current elements, about 100 times

the capacity of current vendor tools. Two-dimensional and three-dimensional electromagnetic field solvers allow extraction of wiring electrical parameters with highly inhomogeneous dielectric environments. Special test devices have been built to capture the relevant aspects of current and future packaging structures and technologies, using time-domain high-speed measurement techniques. GAMMA-Z, a special time-domain technique, allows extraction of broadband transmission line matrix elements for maximum interconnect bandwidths, resulting in realistic card and ceramic interconnect parameter extractions up to 50 GHz.

Signal line traveling through a chip package.

