

CINDY EISNER

EMPLOYMENT

1994-present IBM Haifa Research Laboratory Haifa, Israel

Current position: Senior Architect, Verification Technologies

- Developed a method for functional verification of power gated designs based on sequential equivalence checking; Coordinated the EU FP6 project PROSYD, a €7M project based on the new IEEE standard 1850 PSL (formerly IBM's Sugar) and including eleven industrial, academic and research partners across Europe and Israel; Initiated and led the development of GateAlert, a tool that uses formal techniques to find clock gating opportunities in hardware, now an official part of the IBM chip design methodology; Initiated and participated in an exploratory project to develop a software model checking tool; Led the technical team that developed Sugar 2.0 – the formal specification language selected by the Accellera standards body in April 2002 for IEEE standardization as PSL, and acted as the technical spokesperson for IBM during the language selection process; Developed a method for formal design of hardware control algorithms that has been used in a number of development projects, most recently Waternoose.

1991-1993 Zoran Microelectronics Haifa, Israel

Member, CAD group

- Responsible for introduction of synthesis tools to Zoran, including methodologies for use, integration into design flow, development of supporting toolset, and education of design engineers.

1986-1990 Intel Corporation Haifa, Israel

Member, CAD group

- Wrote the iHDL compiler and C simulation code generator. Later became project leader of the iHDL toolset.

EDUCATION

1982 - 1986 Technion, Israel Institute of Technology Haifa, Israel

B.Sc. Computer Science

1978 - 1980 Princeton University Princeton, New Jersey, USA

Undergraduate studies, Liberal Arts

BOOKS

- C. Eisner and D. Fisman, *A Practical Introduction to PSL*. Springer, 2006.

REFEREED PUBLICATIONS

- C. Eisner, D. Fisman, “Augmenting a Regular Expression-Based Temporal Logic with Local Variables”, to appear in *Proc. 8th International Conference on Formal Methods in Computer Aided Design (FMCAD)*. November 2008.
- C. Eisner, A. Nahir, K. Yorav, “Functional Verification of Power Gated Designs by Compositional Reasoning”, In *Proc. 20th International Conference on Computer Aided Verification (CAV)*, LNCS 5123. July 2008.
- E. Zarpas, C. Eisner, S. Tal, “Policy Validation for System Automation: A Case

Study”, In. *Proc. 9th IEEE International Workshop on Policies for Distributed Systems and Networks*, June 2008.

- E. Arbel, C. Eisner, A. Itskovich, “GateAlert: A Clock Gating Tool”, In. *Proc. 5th Annual Austin Conference on Energy-Efficient Design (ACEED)*. March 2007.
- S. Barner, C. Eisner, Z. Glazberg, D. Kroening, I. Rabinovitz, “ExpliSAT: Guiding SAT-Based Software Verification with Explicit States”, In. *Proc. 2nd Annual Haifa Verification Conference (HVC)*, LNCS 4383. October 2006.
- C. Eisner, D. Fisman, J. Havlicek. A Topological Characterization of Weakness. In *Proc. 24th Annual ACM Symposium on Principles of Distributed Computing (PODC)*, July 2005.
- C. Eisner, “Formal verification of software source code through semi-automatic modeling”. *Software and Systems Modeling (SOSYM)*. 4(1). Springer-Verlag, February 2005.
- C. Eisner, D. Fisman, J. Havlicek, Y. Lustig, A. McIsaac and D. Van Campenhout, “Reasoning with Temporal Logic on Truncated Paths”. In *Proc. 15th Int’l Conference on Computer Aided Verification*, LNCS 2725. Springer, 2003.
- C. Eisner, D. Fisman, J. Havlicek, A. McIsaac and D. Van Campenhout, “The Definition of a Temporal Clock Operator”, In *Proc. 30th International Colloquium on Automata, Languages and Programming (ICALP)*, LNCS 2719. Springer, 2003.
- C. Eisner, "Using Symbolic CTL Model Checking to Verify the Railway Stations of Hoorn-Kersenboogerd and Heerhugowaard". *International Journal on Software Tools for Technology Transfer (STTT)*, 4(1). Springer, 2002.
- C. Eisner, "Model checking the garbage collection mechanism of SMV". In *Electronic Notes in Theoretical Computer Science*, Vol. 55, No. 3. Elsevier Science Publishers, 2001.
- I. Beer, S. Ben-David, C. Eisner, D. Fisman, A. Gringauze and Y. Rodeh, "The Temporal Logic Sugar". In *Proc. 13th International Conference on Computer Aided Verification (CAV)*, LNCS 2101. Springer, 2001.
- I. Beer, S. Ben-David, C. Eisner and Y. Rodeh, "Efficient Detection of Vacuity in Temporal Model Checking". *Formal Methods in System Design*, Vol. 18, No. 2. Kluwer Academic Publishers, 2001.
- C. Eisner, R. Hoover, W. Nation, K. Nelson, I. Shitsevalov, K. Valk, “A Methodology for Formal Design of Hardware Control with Application to Cache Coherence Protocols”. In *Proc. 37th Design Automation Conference (DAC)*. Association for Computing Machinery, Inc. June 2000.
- C. Eisner, “Using Symbolic Model Checking to Verify the Railway Stations of Hoorn-Kersenboogerd and Heerhugowaard”. In *Proceedings 10th IFIP WG10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods (CHARME)*, LNCS 1703. Springer 1999.
- I. Beer, S. Ben-David, C. Eisner, Y. Rodeh, “Efficient Detection of Vacuity in ACTL Formulas”. In *Proceedings 9th International Conference on Computer Aided Verification (CAV)*, LNCS 1254. Springer 1997.
- I. Beer, S. Ben-David, C. Eisner, D. Geist, L. Gluhovsky, T. Heyman, A. Landver, P. Paanah, Y. Rodeh, G. Ronin, Y. Wolfsthal, "RuleBase: Model Checking at IBM", In *Proceedings 9th International Conference on Computer Aided Verification (CAV)*, LNCS 1254. Springer, 1997.
- I. Beer, S. Ben-David, C. Eisner, A. Landver, “RuleBase: an Industry Oriented Formal Verification Tool”, in *Proceedings 33rd Design Automation Conference (DAC)*. Association for Computing Machinery, Inc. June 1996.

INVITED TALKS AND PAPERS

- C. Eisner, “PSL for Runtime Verification: Theory and Practice”, In *Proc. 7th Workshop on Runtime Verification (RV)*, LNCS 4839. March 2007.
- C. Eisner, Invited speaker on the topic of “Coordinating a European Project” at ISERD (Israeli-Europe R&D Directorate for the EU Framework Program) Information Day, February 2007.
- C. Eisner, Invited talk titled “Sweet and sour: adventures in the development of a property specification language” at the 2nd Annual Haifa Verification Conference, October 2006.
- C. Eisner, Invited talk titled “Semantic issues in the definition of a hardware specification language” at Workshop on Semantics and its Applications, Tel Aviv University, December 2005.
- C. Eisner, Invited talk titled “Reasoning About Multiply-Clocked Hardware” at Workshop on Semantics and Verification of Hardware and Software Systems, Tel Aviv University, May 2003.
- S. Ben-David, C. Eisner, D. Geist and Y. Wolfsthal, “Model Checking at IBM”. *Formal Methods in System Design*, 22(2), Kluwer Academic Publishers, 2003.
- C. Eisner and D. Peled, "Comparing Symbolic and Explicit Model Checking of a Software System". In *Proc. 9th International SPIN Workshop on Model Checking of Software*, LNCS 2318, Springer, 2002.
- C. Eisner and D. Fisman, "Sugar 2.0 Proposal Presented to the Accellera Formal Verification Technical Committee", March 2002. At: http://www.haifa.il.ibm.com/projects/verification/sugar/Sugar_2.0_Accellera.ps
- Invited speaker, 6th International Workshop on Formal Methods for Industrial Critical Systems (FMICS), July 2001
- Y. Abarbanel-Vinov, N. Aizenbud-Reshef, I. Beer, C. Eisner, D. Geist, T. Heyman, I. Reuveni, E. Rippel, I. Shitsevalov, Y. Wolfsthal and T. Yatzkar-Haham, "On the Effective Deployment of Functional Formal Verification". *Formal Methods in System Design*, 19(1), Kluwer Academic Publishers, 2001.

TECHNICAL REPORTS

- C. Eisner, D. Fisman, “Proposal for Extending Annex B of PSL with Local Variables, Procedural Blocks, Past Expressions and Clock Alignment Operators”, IBM Research Report H-0256, January 2008.
- C. Eisner, D. Fisman, J. Havlicek, J. Mårtensson, “The \top, \perp Approach for Truncated Semantics”, Accellera Technical Report 2006.01, May 2006.
- J. Havlicek, D. Fisman and C. Eisner, “Basic Results on the Semantics of Accellera PSL 1.1 Foundation Language”, Accellera Technical Report 2004.02, May 2004.

PATENTS AND PATENTS PENDING

- C. Eisner, K. Yorav, “Functional Verification of Power Gated Designs by Compositional Reasoning”, US Patent Application Number 12/174650, filed July 2008.
- E. Arbel, C. Eisner, O. Fuhrmann, A. Itskovich, D. Levitt, “Devices and Methods to Cluster Boolean Functions for Clock Gating”, US Patent Application Number 12/053384, filed March 2008.
- S. Ruah, S. Keidar-Barner, C. Eisner, T. Veksler, O. Shacham, “Device, System and Method for Formal Verification”, US Patent Application Number 11/845118, filed August 2007.
- C. Eisner, I. Itskovich, I. Berger and D. Ramon, “Over Approximation of

Integrated Circuit Based Clock Gating”, US Patent Application Number 11/836160, filed August 2007.

- C. Eisner, N. Maeding, A. Itskovich and E. Arbel, “Circuit Design Optimization of Integrated Circuit Based Clock Gated Memory Elements”, US Patent Application Number 11/773412, filed July 2007.
- C. Eisner and A. Itskovich, “Apparatus for and Method of Estimating the Quality of Clock Gating Solutions for Integrated Circuit Design”, US Patent Application Number: 11/755015, filed May 2007.
- I. Beer and C. Eisner, “Automatic Abstraction of Software Source Code”, U.S. patent No. 7,146,605. December 2006.
- Z. Glazberg, I. Rabinovitz, S. Barner and C. Eisner, “Software Verification Using Hybrid Explicit and Symbolic Model”, US Patent Application Number: 11/329535, filed January 2006.
- C. Eisner and M. Farkash, “A Method for Multi-Cycle Clock Gating”, US Patent Application Number: 11/311756, filed December 2005.
- C. Eisner, P. Hofstee, D. Stasiak and A. Itskovich, “Clock Gating Through Data Independent Logic”, US Patent Application Number: 11/295936, filed December 2005.
- I. Beer, C. Eisner, Y. Rodeh, “Method and system for reducing state space variables prior to symbolic model checking”. U.S. patent No. 6,192,505. February 2001.

AWARDS RECEIVED

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| 2006 | ■ IBM Bravo! Award for: Extraordinary Contribution to PROSYD. |
| 2005 | ■ IBM Outstanding Innovation Award for: The PSL/Sugar Standard: Fulfillment and Impact.
■ IEEE-SA Standards Board Award for Contribution to IEEE-1850. |
| 2002 | ■ IBM Outstanding Innovation Award for: Formulation of the Sugar specification language and its selection as an industry standard. |
| 2001 | ■ IBM Outstanding Technical Achievement Award for: Development of a methodology for formal protocol design and verification and its successful deployment in Netfinity and AS/400 Products. |
| 1999 | ■ IBM Research Division Award for: Leading the architecture level formal verification of the Coosa system. |
| 1997 | ■ IBM Research Division Award for: Contribution to formal verification at IBM. |
| 1995 | ■ IBM Research Division Award for: Contribution to model checking technology and RuleBase system.
■ IBM Market Driven Quality Award. |
| 1988 | ■ INTEL Achievement Award for: Outstanding contribution to the team that developed state-of-the-art behavioral structural definition language for logic design. |

PROGRAM COMMITTEES

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| 2007 | ■ Program committee member, 7th Int’l Conference on Formal Methods in Computer-Aided Design (FMCAD) |
| 2005 | ■ Program committee member, 11th Int’l Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS) |
| 2003 | ■ Organizing committee member, Workshop on Semantics and Verification of Hardware and Software Systems |
| 2002 | ■ Program committee member, Formal Methods Europe (FME) |

STANDARDS COMMITTEES

- 2004-present ■ Working Group Member, IEEE-1850 (PSL)
- 2000-2004 ■ Member, Accellera Formal Verification Technical Committee
- 2000-2004 ■ Member, Accellera SystemVerilog Assertions Sub-Committee

MISCELLANEOUS

- 2005 ■ Proposal reviewer for Israel Science Foundation (ISF)
- 2002 ■ International referee for Council of Physical Sciences of the Netherlands Organization for Scientific Research (NWO)