Bang-Bang Digital PLLs at 11 GHz and 20 GHz with sub-200-fs Integrated Jitter for High Speed Serial Communication Applications

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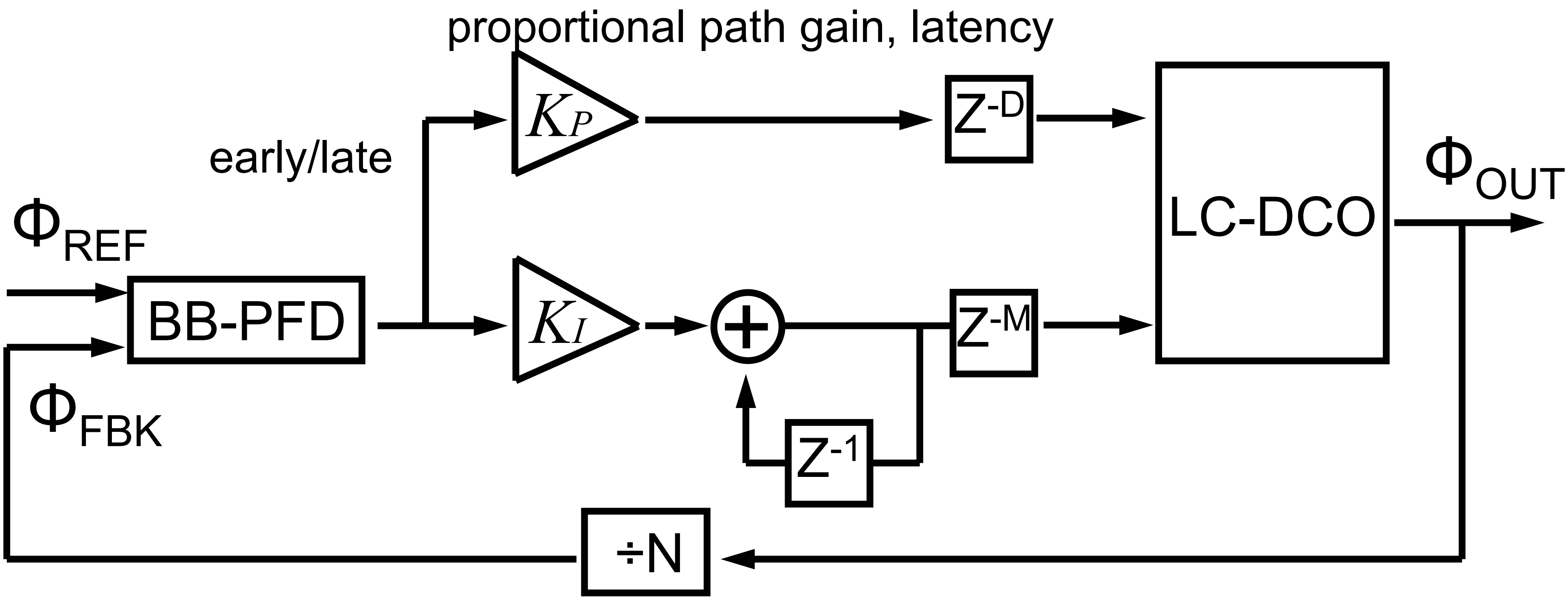
Motivation

- Goal: demonstrate DPLL adequate for 8- to 11-Gbps and 17- to 20-Gbps wireline communication applications:
  - jitter (integrated from fc/1667 to fc/2) ~ 0.3 ps rms
  - bandwidth: ~ 1 MHz
  - integer-N: ~ 40
- A drop-in replacement for analog PLLs, offering:
  - significant area savings
  - increased programmability
  - reduced analog content (models, variability, sensitivity)
  - portability to advanced CMOS technologies

Bang-bang DPLL Background



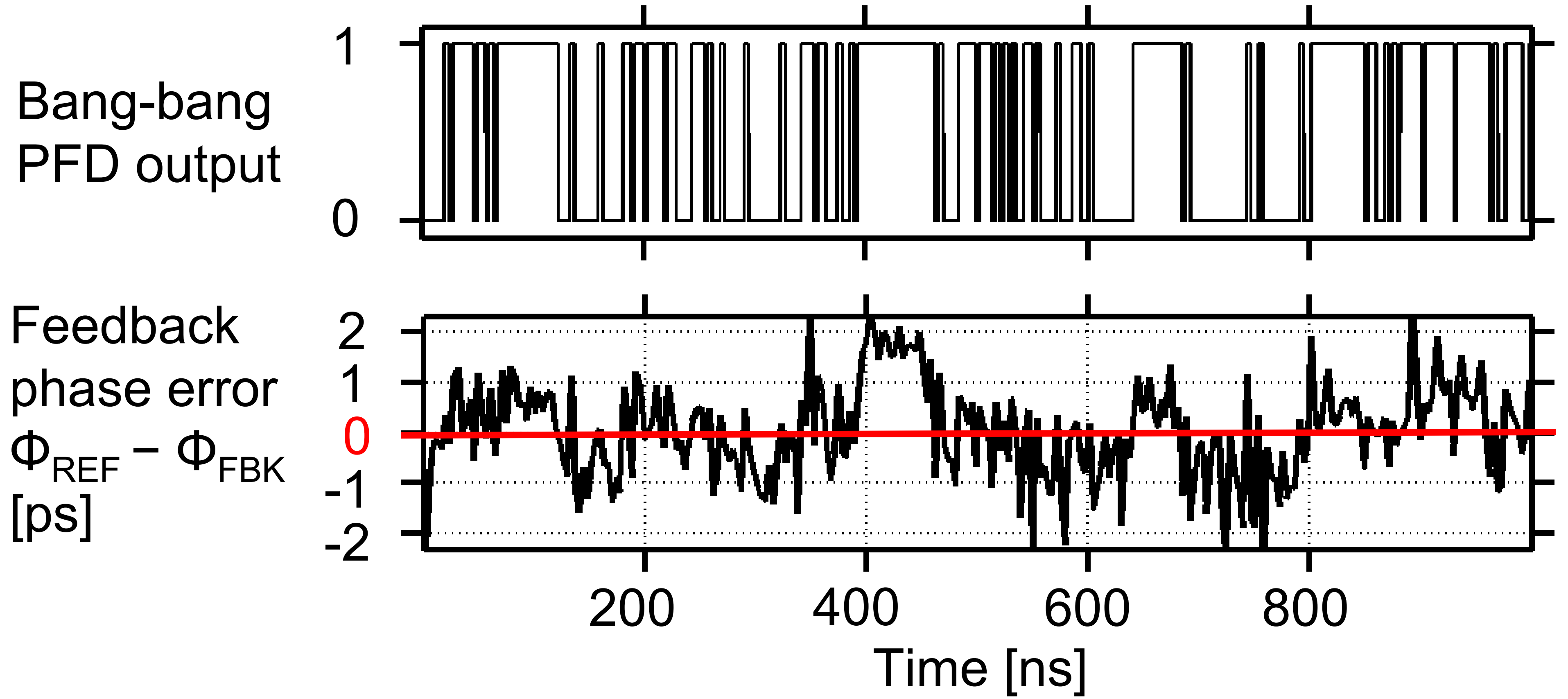
Main design considerations:

- PFD: bang-bang or TDC
- Loop Filter: BB-PLL jitter grows with increase in proportional path gain (K_P) and latency (D)*
- DCO: tuning range, fine tuning step (K_{DCO}), phase noise

* Walker 1992, Da Dalt 2005, Hanumolu 2007

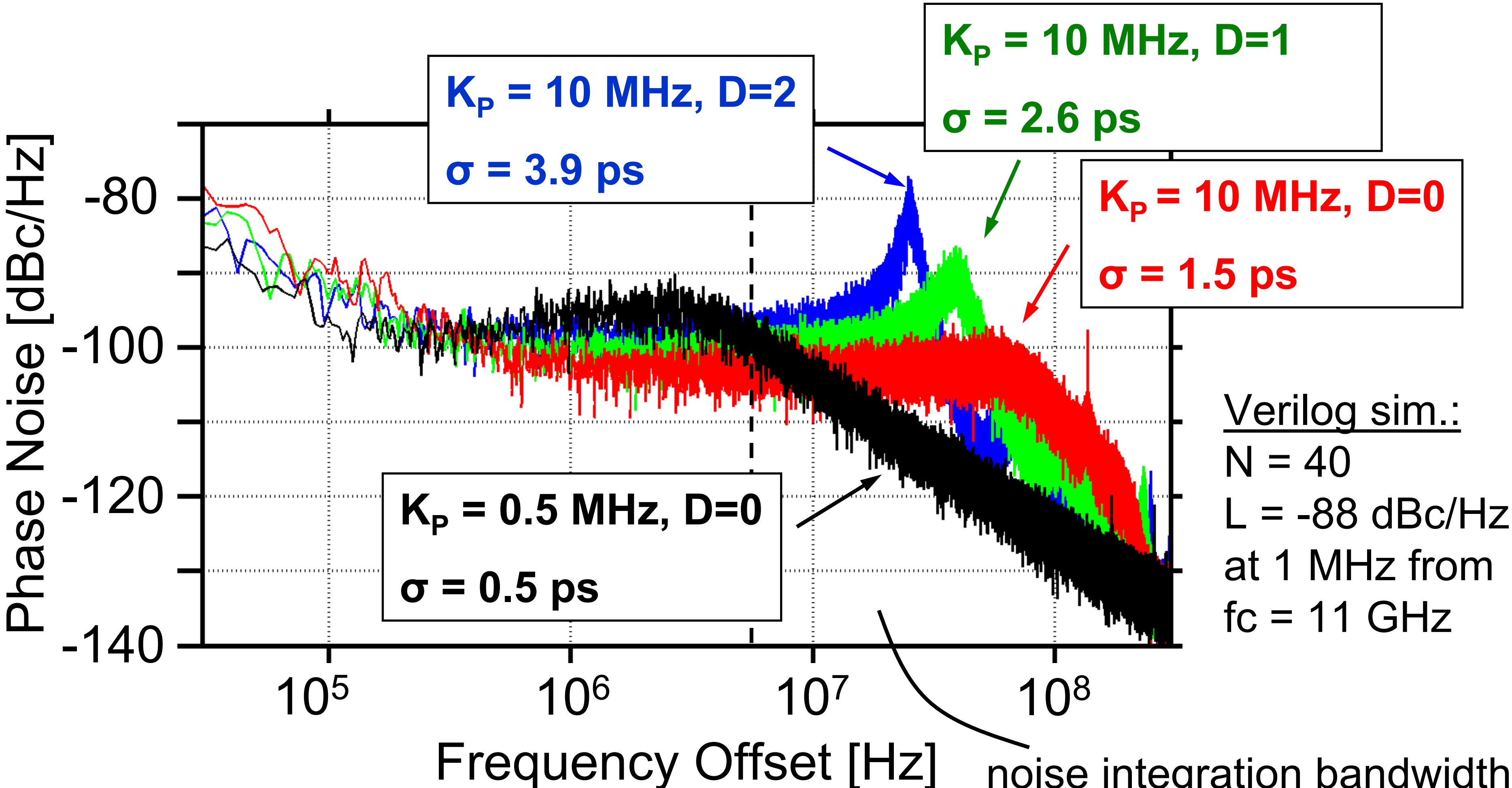
Bang-bang PFD vs TDC

Integer-N LC-DPLL Verilog simulation results



- Bang-bang PFD produces <u>same output</u> as 2 ps resolution TDC
- Need sub-1ps resolution TDC to extract significantly more information than provided by BB-PFD

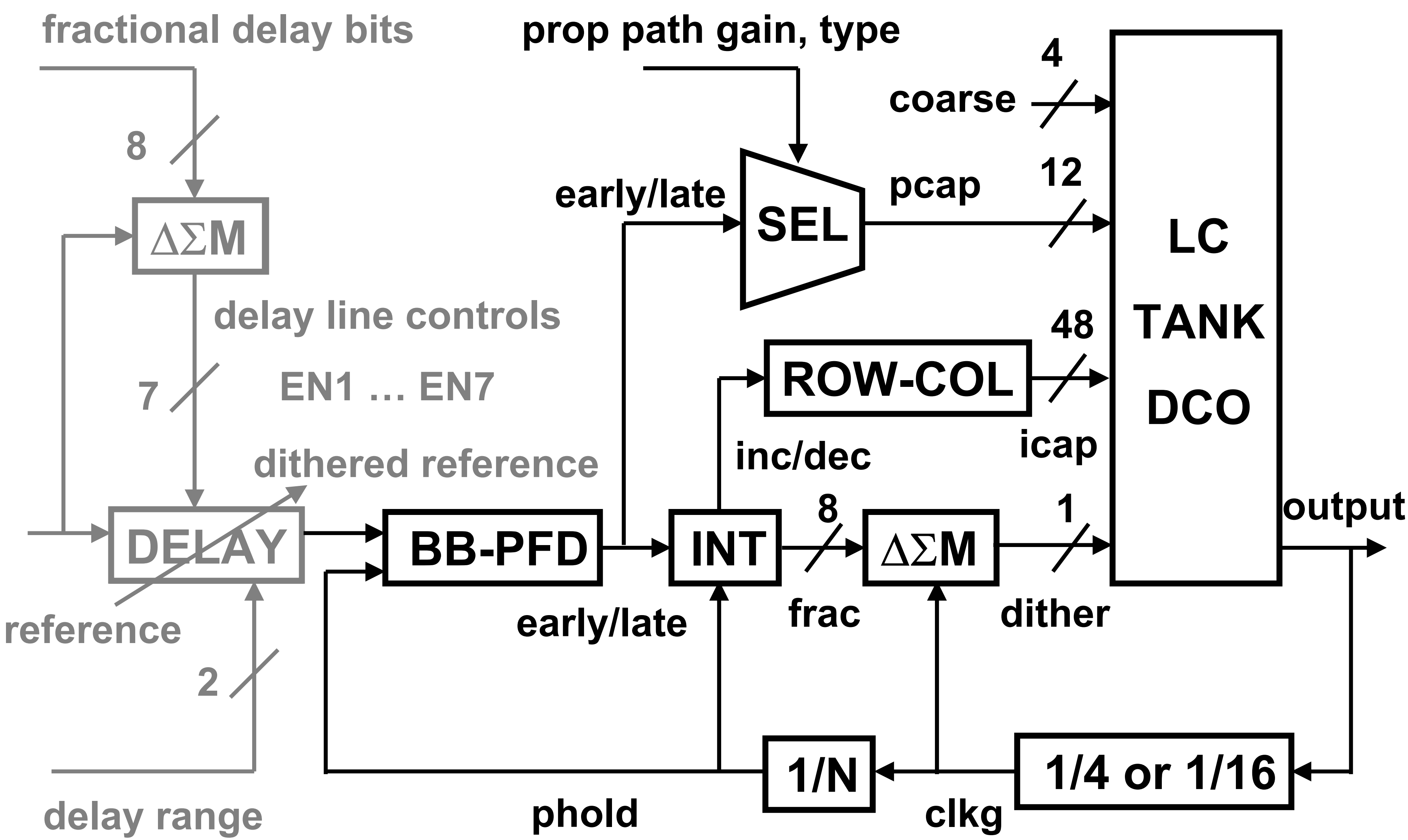
Proportional Path Latency and Gain



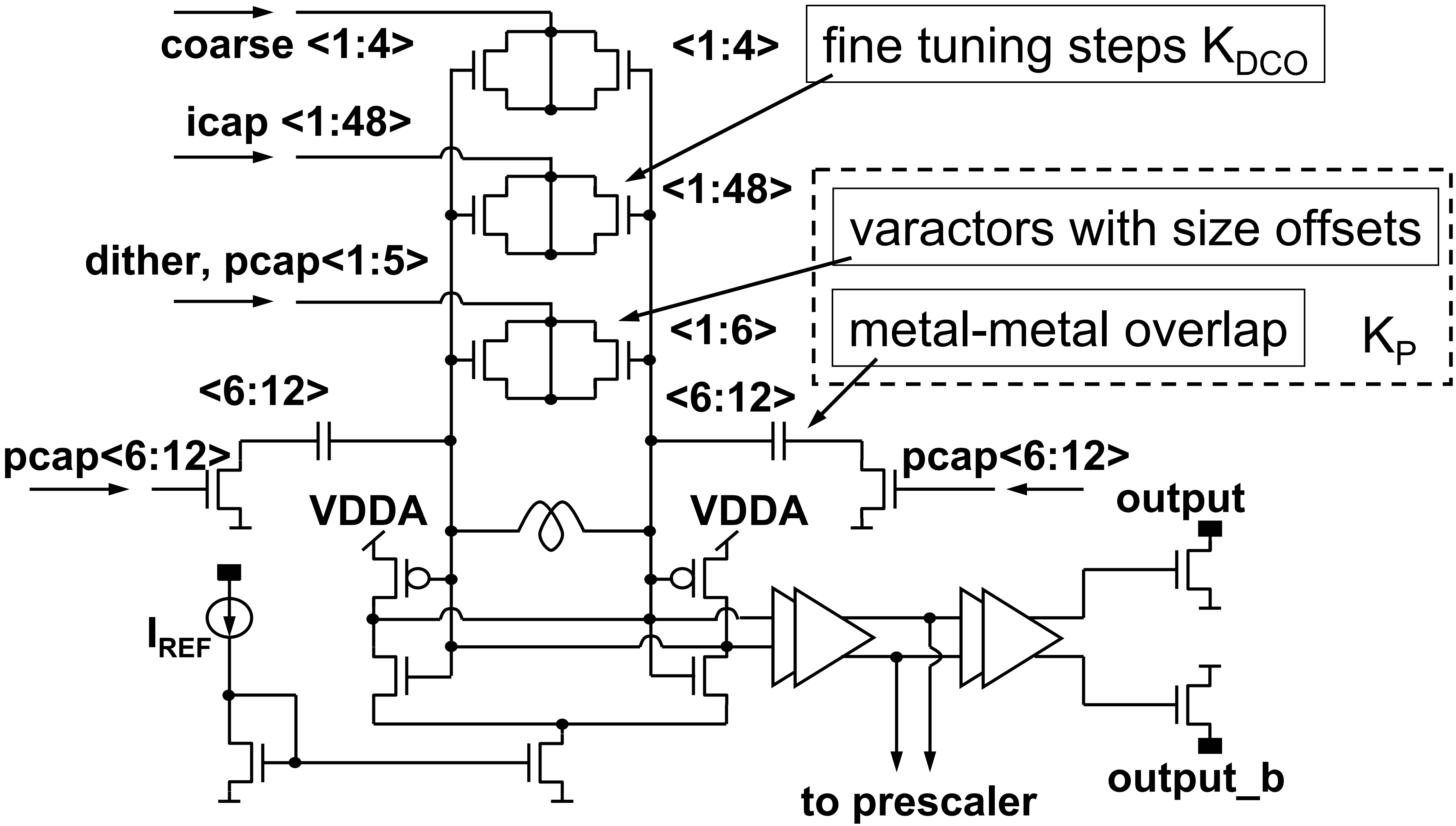
- Latency (D) of the proportional path should be minimized
- Gain of the proportional path (K_P) should be reduced

⇨Gain of the integral path needs to be significantly reduced to keep the loop stable

BB-DPLL Block Diagram



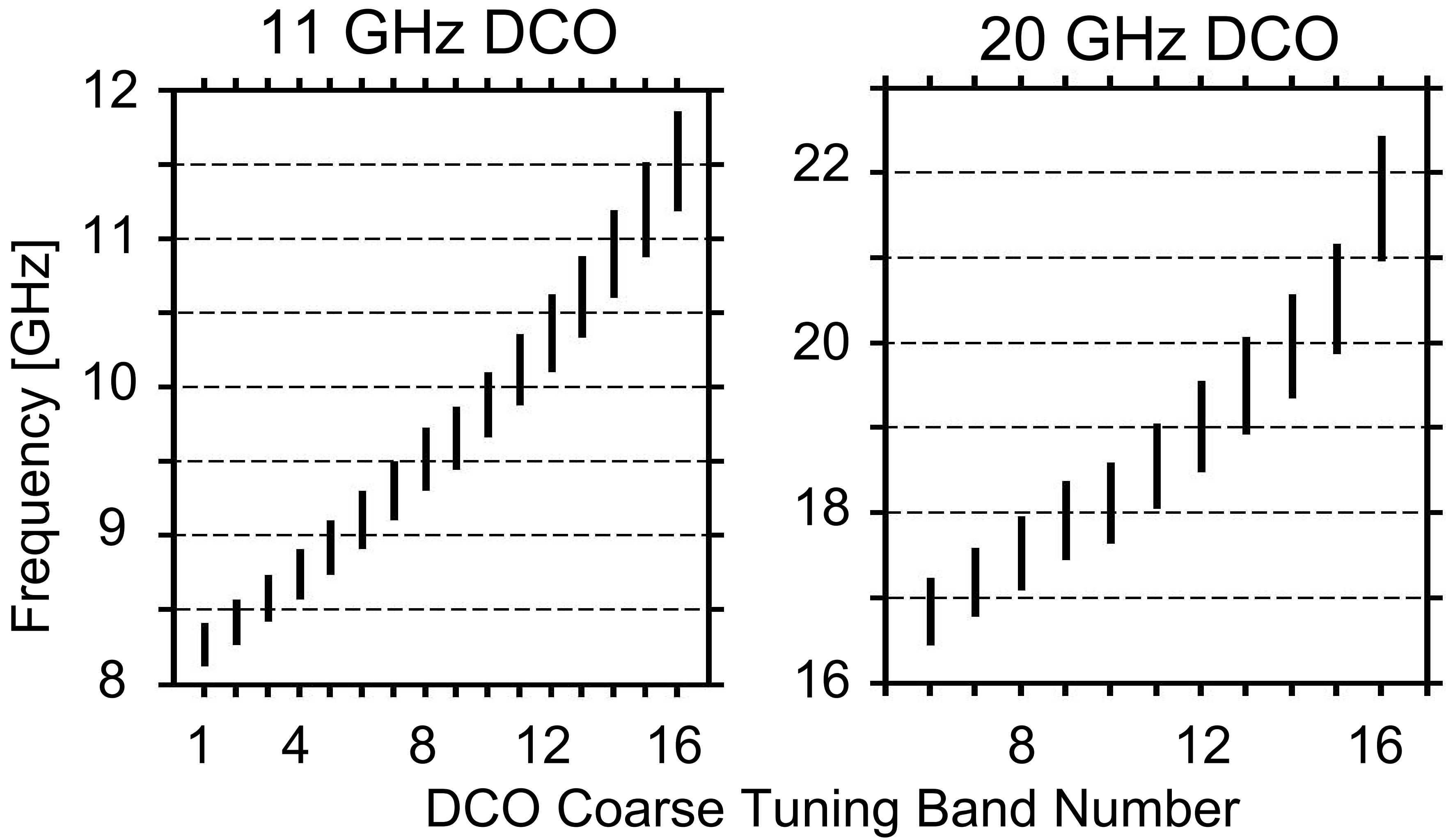
11 GHz, 20 GHz LC DCO Topology



<u>Main design challenges:</u>

- preserving oscillator Q while meeting tuning range and K_{DCO} requirements
- realizing low-gain K_P

LC-DCO Coarse Band Tuning Ranges

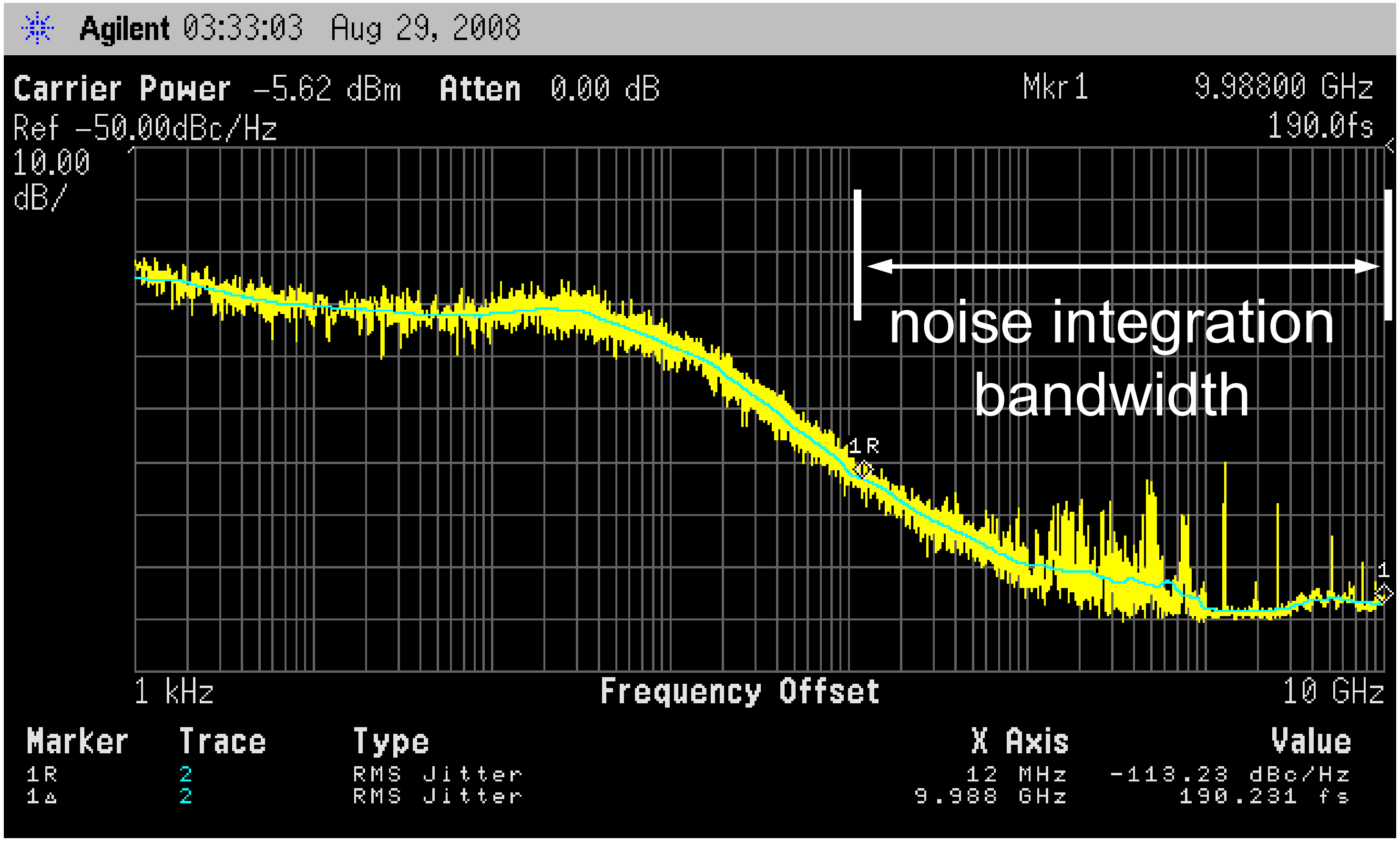


K_{DCO} = 6 MHz − 14 MHz

K_{DCO} = 16 MHz − 30 MHz

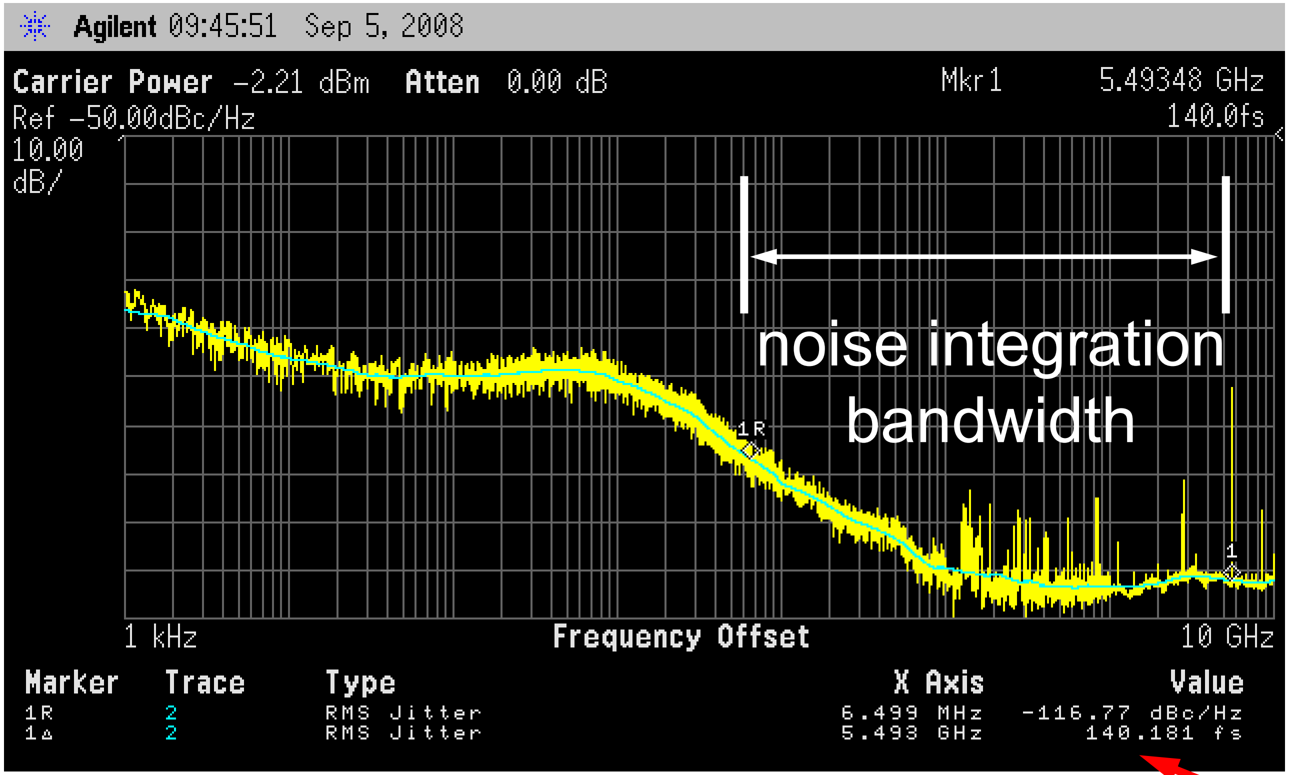
- The oscillators meet tuning range and K_{DCO} requirements

20 GHz BB-DPLL Phase Noise



- fc = 20.08 GHz, N=80 (251 MHz reference), no reference dithering
- RMS Jitter: 190 fs (12 MHz to 10 GHz)
- Proportional path: switched metal-metal overlap capacitance

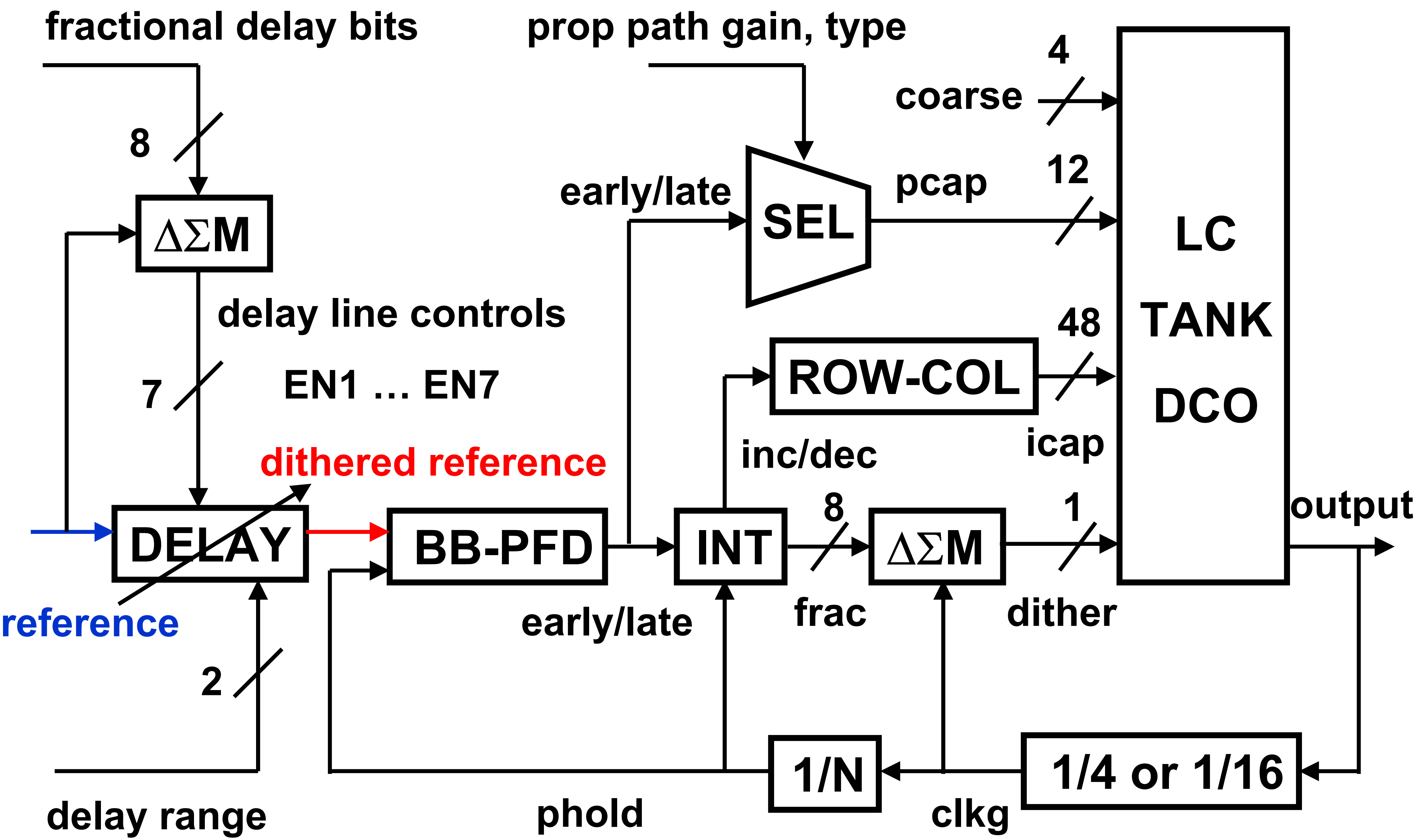
11 GHz BB-DPLL Phase Noise and Jitter



pcap	K_P [MHz]	RMS Jitter [fs]
6	4.65	1140
7	2.0	664
8	0.83	375
9	0.35	208
10	0.15	152
11	0.15	145
12	0.15	140

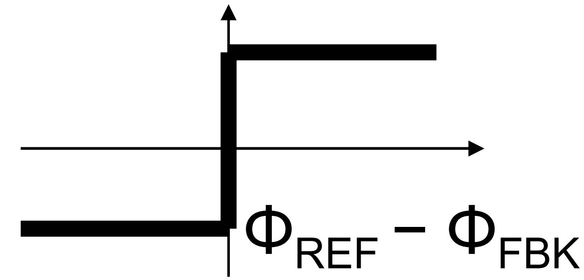
- fc = 11 GHz, N=40 (275 MHz reference), no reference dithering
- RMS Jitter: 140 fs (6.5 MHz to 5.5 GHz); 345 fs (1 kHz to 10 GHz)
- Proportional path: switched metal-metal overlap capacitance **pcap<12>** (similar results for nFET in nwell varactors with size offsets **pcap<1:5>**)

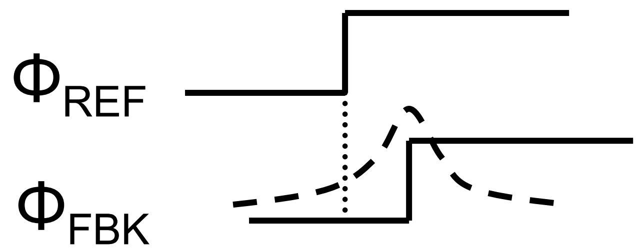
BB-DPLL Block Diagram



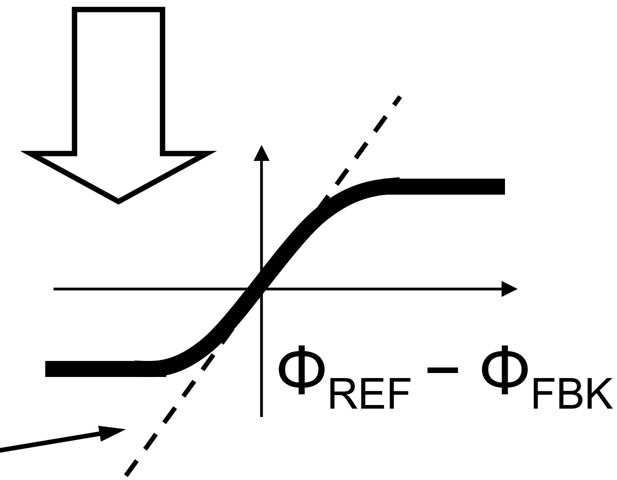
BB-PFD Linearization and Gain

Original non-linear transfer function:





Linearized transfer function:



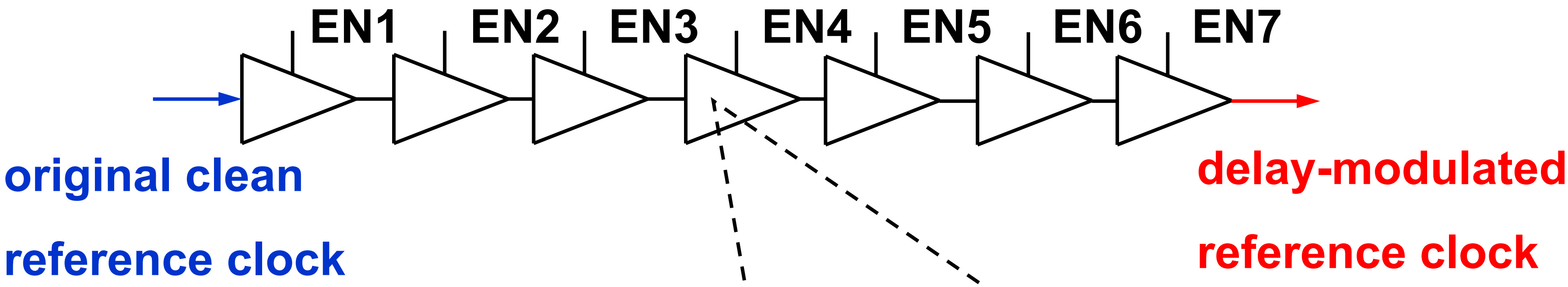
$$K_{PFD} = \frac{1}{\sqrt{2\pi}} \frac{1}{\sigma_{IN}}$$

Lee 2004

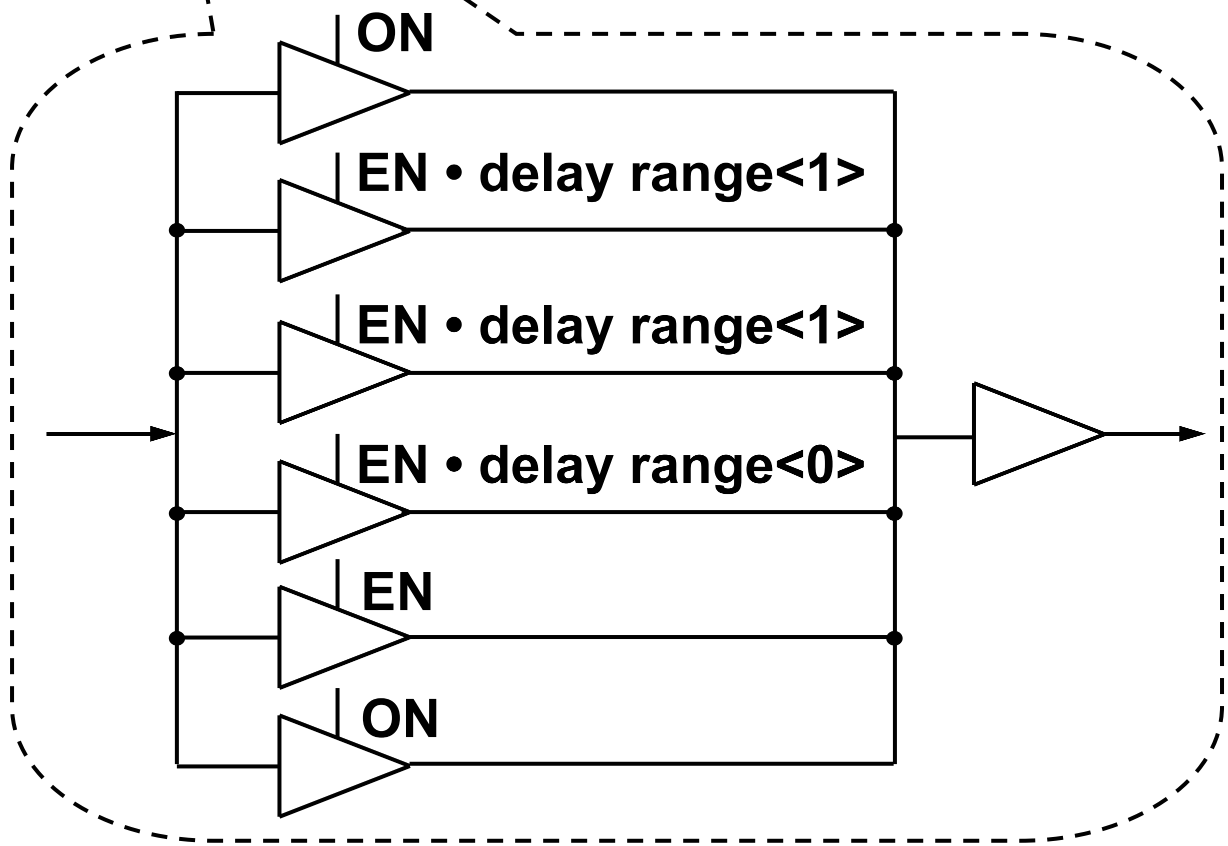
Da Dalt 2006

- BB-PFD gain is inversely proportional to input jitter
- Low-noise BB-DPLL will have non-linear dynamics

Variable Delay Line



delay per stage		
delay range	sim. [ps]	meas. [ps]
11	1.7	1.4
10	4.0	3.4
01	7.6	6.1
00	14.1	11.4

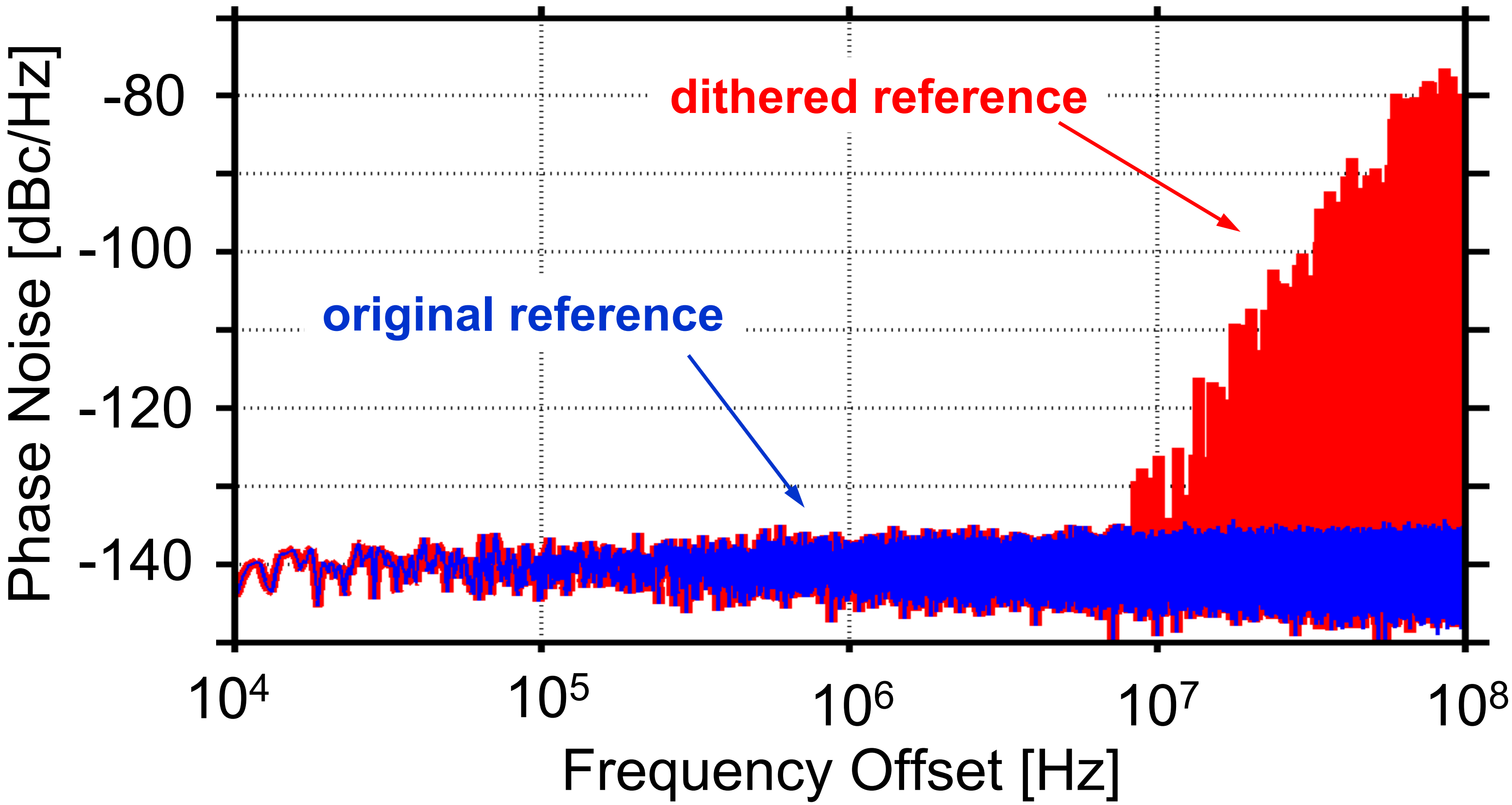


- Identical delay cells enable high-order ΔΣ modulation

Reference Clock Dithering Simulation

original reference: flat -140 dBc/Hz phase noise floor

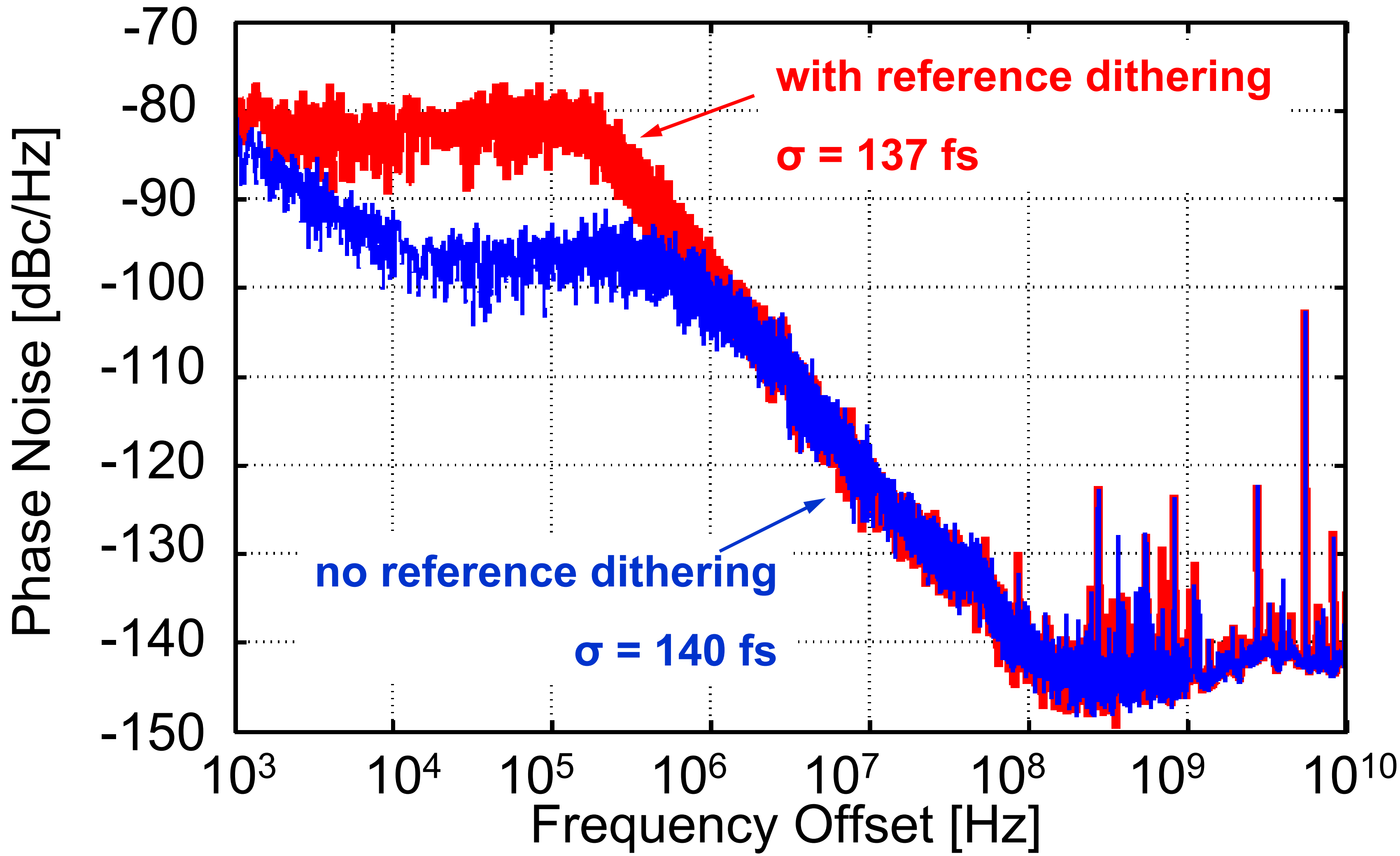
dithered reference: 3rd order ΔΣ modulated (10 ps per delay stage)



- High reference jitter achieved without adding in-band noise
- Effective DPLL linearization, loop bandwidth control

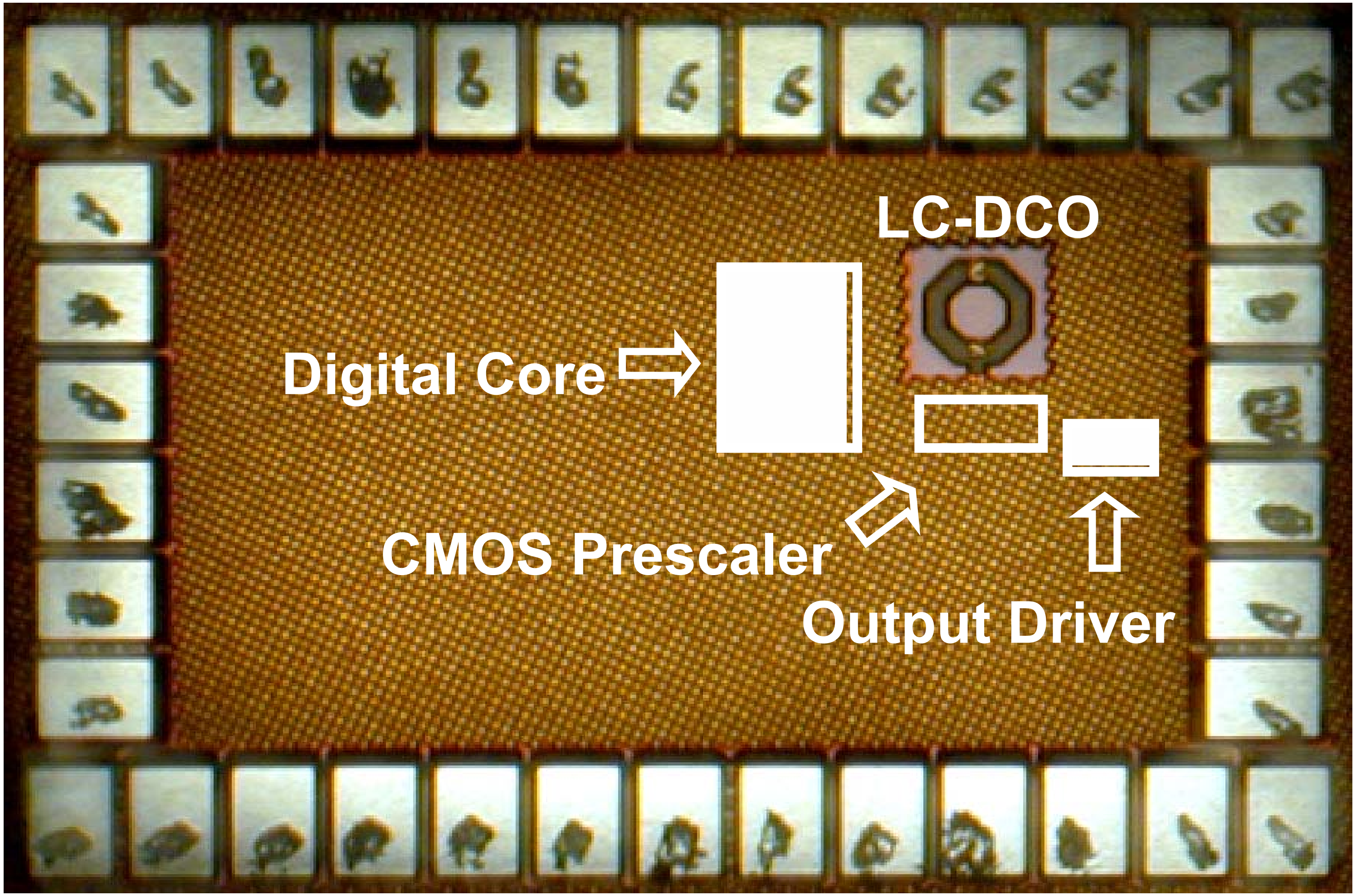
Measured 11 GHz Phase Noise Plots

VDDA=1.2V (17mA), VDD=1.1V (9.2mA), N = 40 (275 MHz reference)



- DPLL bandwidth control by proportional path gain or by reference dithering
- Reference dithering does not degrade the RMS jitter σ (6.5 MHz to 5.5 GHz)

11 GHz BB-DPLL Die Photograph



pad pitch: 100 μm

- DPLL area can be improved with more efficient layout

BB-DPLL Performance Summary

		11 GHz	20 GHz
CMOS Technology		65 nm bulk	
Area		410 μm × 215 μm	425 μm × 265 μm
Voltages, Currents	Digital Core	1.1 V, 9.1 mA	1.1 V, 4.5 mA
	DCO, Prescalers	1.2 V, 17 mA	1.6 V, 37 mA
Total Power Dissipation		31 mW	64 mW
Tuning Range		8.1 – 11.8 GHz	16.4 – 22.4 GHz
RMS Jitter (fc/1167 – fc/2)		138 fs [1,2]	190 fs
RMS Jitter (1MHz – 10 GHz)		345 fs [3]	962 fs
Phase Noise (at 10 MHz offset)		-121 dBc/Hz	-112 dBc/Hz

[1] RMS jitter (6.5 MHz to 5.5 GHz) measured at 14 points across the 10.64 GHz to 11.16 GHz band (in 1 MHz reference steps) was under 178 fs.

[2] at T = 125°C, 8.4 GHz the RMS jitter (5 MHz to 4.2 GHz) was 205 fs.

[3] n-cycle jitter under 0.8 ps RMS
(from 1-cycle to 1024-cycle; oscilloscope noise floor ~ 450 fs)

Conclusion

- Integer-N BB-DPLLs at 11 GHz and 20 GHz meet integrated jitter and bandwidth requirements of high-speed serial communication applications.
- Key design features:
  - low-gain low-latency proportional path control is directly applied to the DCO
  - two different implementation types of DCO proportional controls demonstrated.
- Time-domain reference dithering technique with noise shaping to effectively control BB-DPLL bandwidth demonstrated.