

# 96 GHz Static Frequency Divider in SiGe bipolar technology

Alexander Rylyakov and Thomas Zwick

IBM T.J. Watson Research Center

November 12, 2003

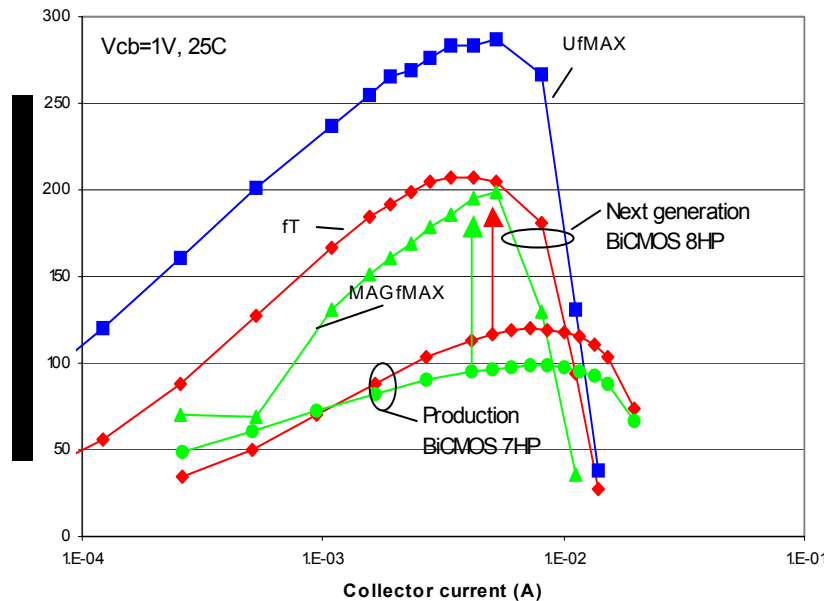
# Outline

- Review of previous 0.13  $\mu\text{m}$  SiGe results:
  - 4.2 ps Ring Oscillators
  - 100 GHz Dynamic Divider
  - 62 GHz ECL Static Divider
- Design of the 96 GHz E<sup>2</sup>CL Static Divider
- Test Setup and Measurement Results
- 0.13  $\mu\text{m}$  and 0.18  $\mu\text{m}$  SiGe Dividers  
Performance Summary and Conclusion

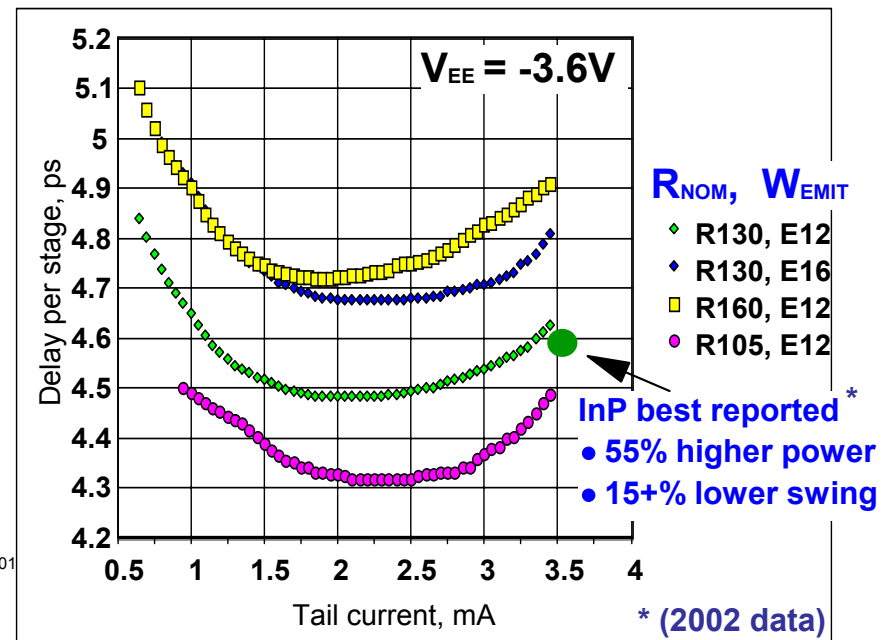
# SiGe8HP Technology Overview and Ring Oscillators

- Cutoff frequency +75% from prior generation: > 200 GHz  $f_T$
- Power gain cutoff frequency +80% from prior generation:
  - ▶  $f_{MAX}(MAG) > 180\text{GHz}$  and  $f_{MAX}(U) > 250\text{ GHz}$
- Record RO delays: < 50% of prior generation
- Experimental SiGe9HP development wafer achieves 3.9 ps

$f_T, f_{MAX}$  vs.  $I_C$



RO delay vs. tail current



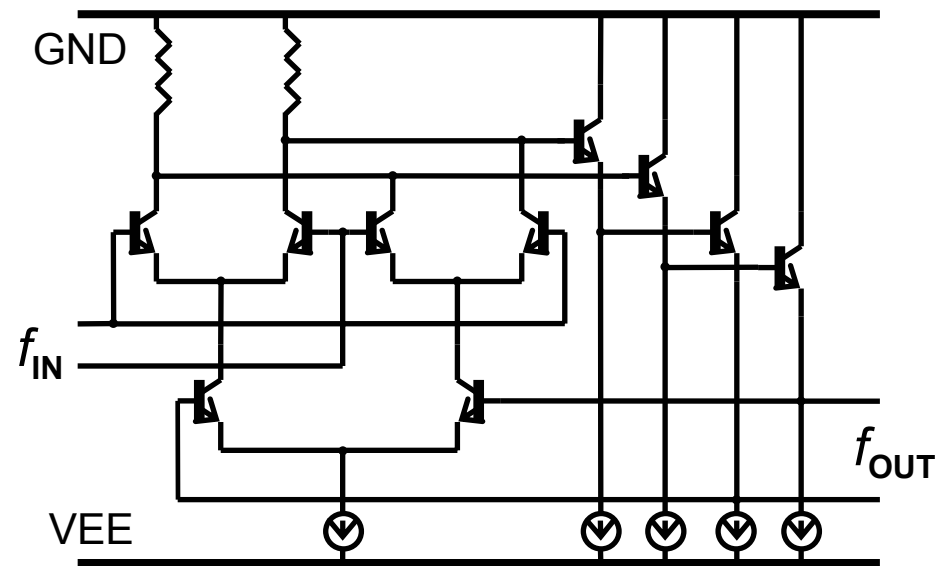
# SiGe8HP Dynamic Frequency Divider

## ■ Record Performance:

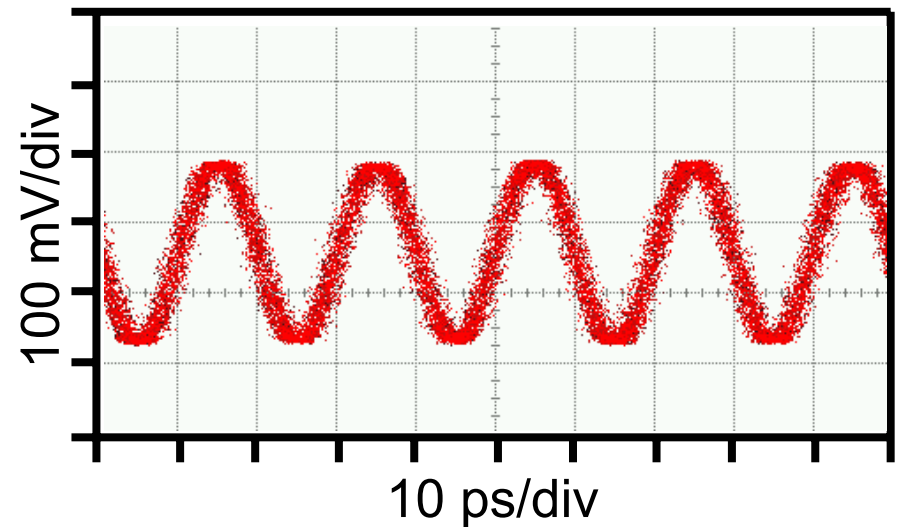
- ▶ 100 GHz, 285mW at -3.8V
- ▶ outputs 260 mVpp single-ended at 50 GHz
- ▶ packaged and tested by SHF (Electronics Letters, Jan 2003)

## ■ Competition (published results):

- ▶ Hitachi: SiGe, 82 GHz, 396mW at -5.2V, used divide by 4 (ISSCC 2000)
- ▶ NTT: InP/InGaAs HBTs, 90 GHz, 1.4W total at -5.5V, used divide by 8, claim 110mW per flip-flop (IPRM 2002)



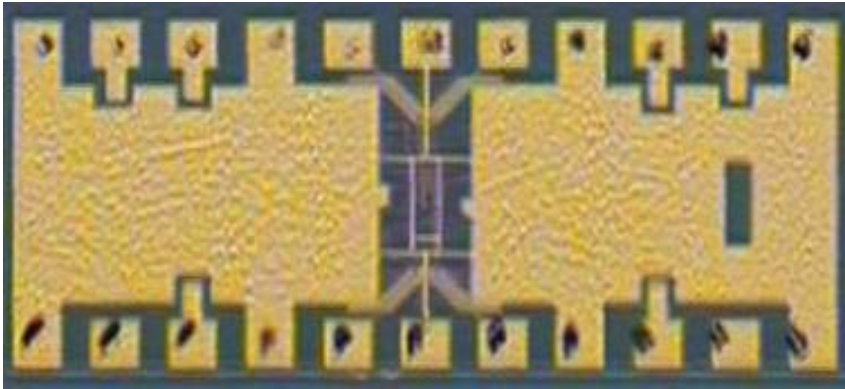
Dynamic divider circuit diagram



Output 50 GHz signal at 100 GHz input

# SiGe8HP ECL Static Frequency Divider

- Maximum input frequency: 62 GHz, at -3.8V
- Close to 2x increase in performance (compared to same design in SiGe7HP)
- Power dissipation can be traded off for performance



Die micrograph

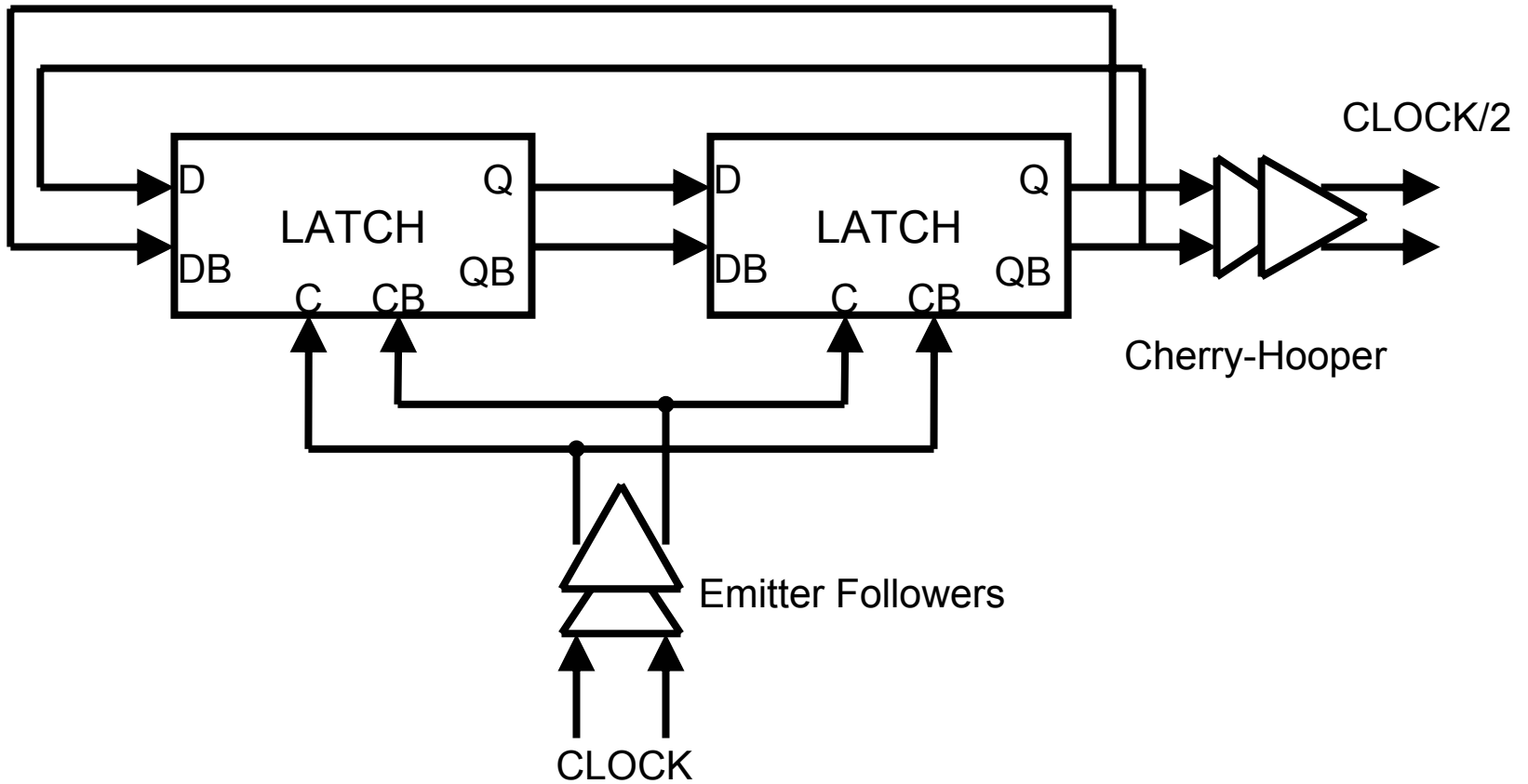
V <sub>ee</sub> = - 3V, P <sub>in</sub> = 0 dBm	
tail current ( mA )	max frequency ( GHz )
2.8	60
1.0	49
0.8	45
0.4	30

Power-speed tradeoff

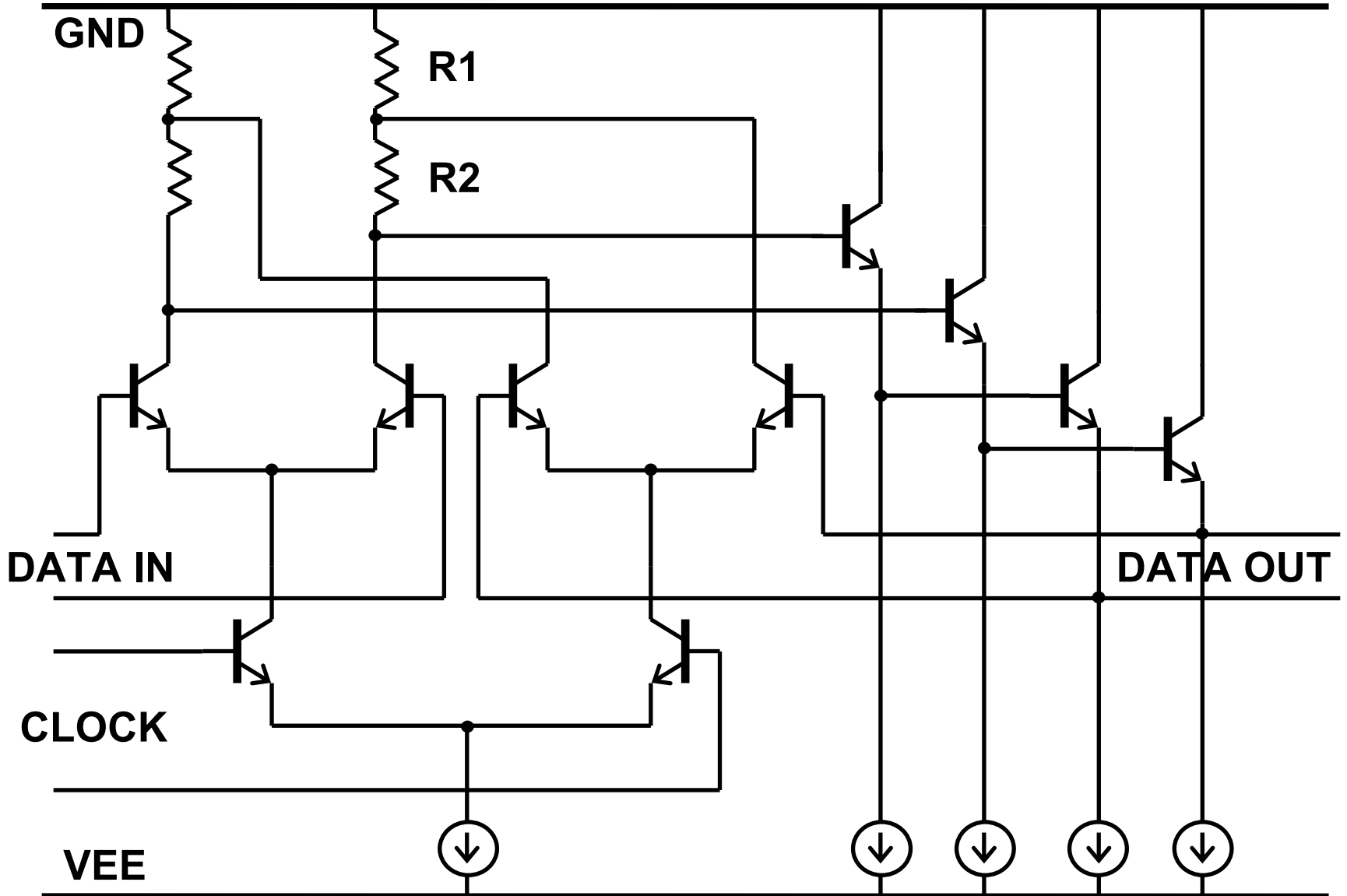
# Design of the 96 GHz E<sup>2</sup>CL Static Divider

- Motivation:
  - explore performance limits of 0.13 um SiGe (“SiGe8HP”)
  - compare design approaches (ECL vs E<sup>2</sup>CL)
  - develop test equipment (dividers are useful for synchronization)
- Design Overview:
  - fully static, double emitter follower design
  - no inductive peaking
  - input clock signal is not amplified, only down-shifted using emitter followers
  - output clock buffer is a Cherry-Hooper amplifier

# Block Diagram of the Design

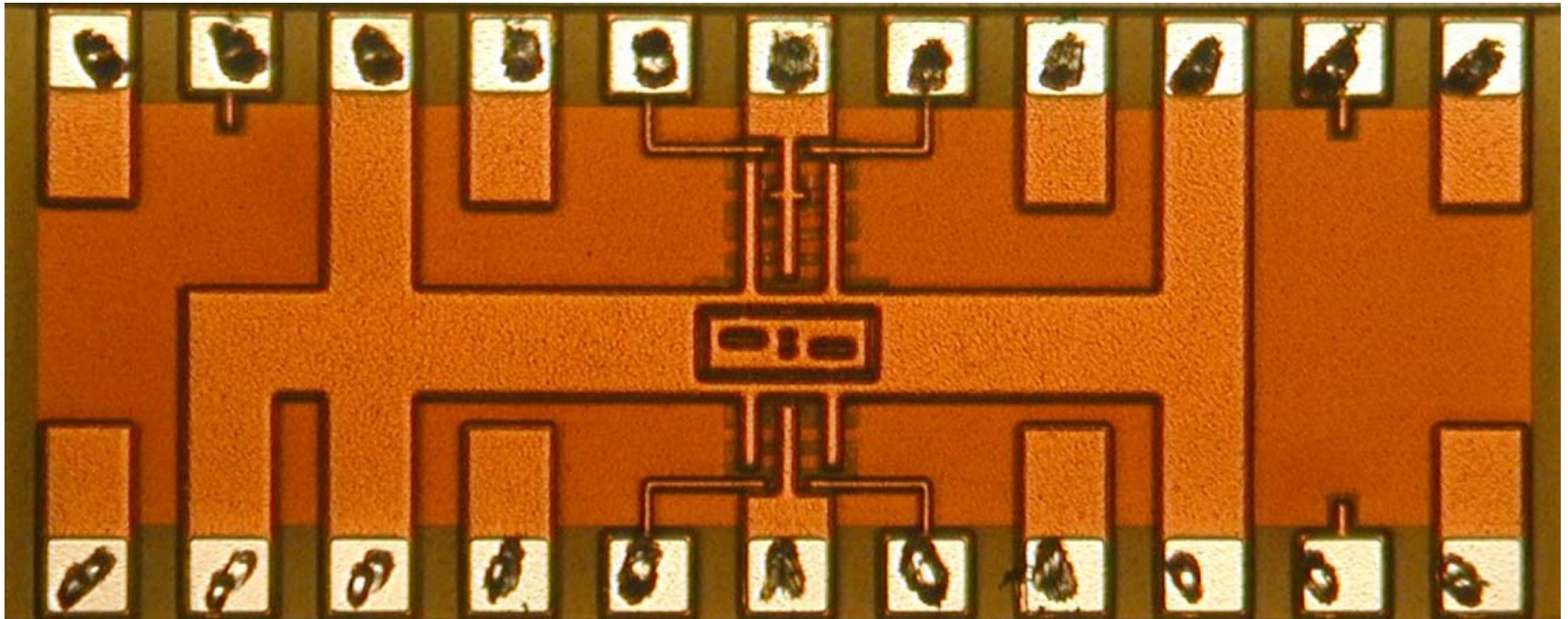


# Latch Schematic



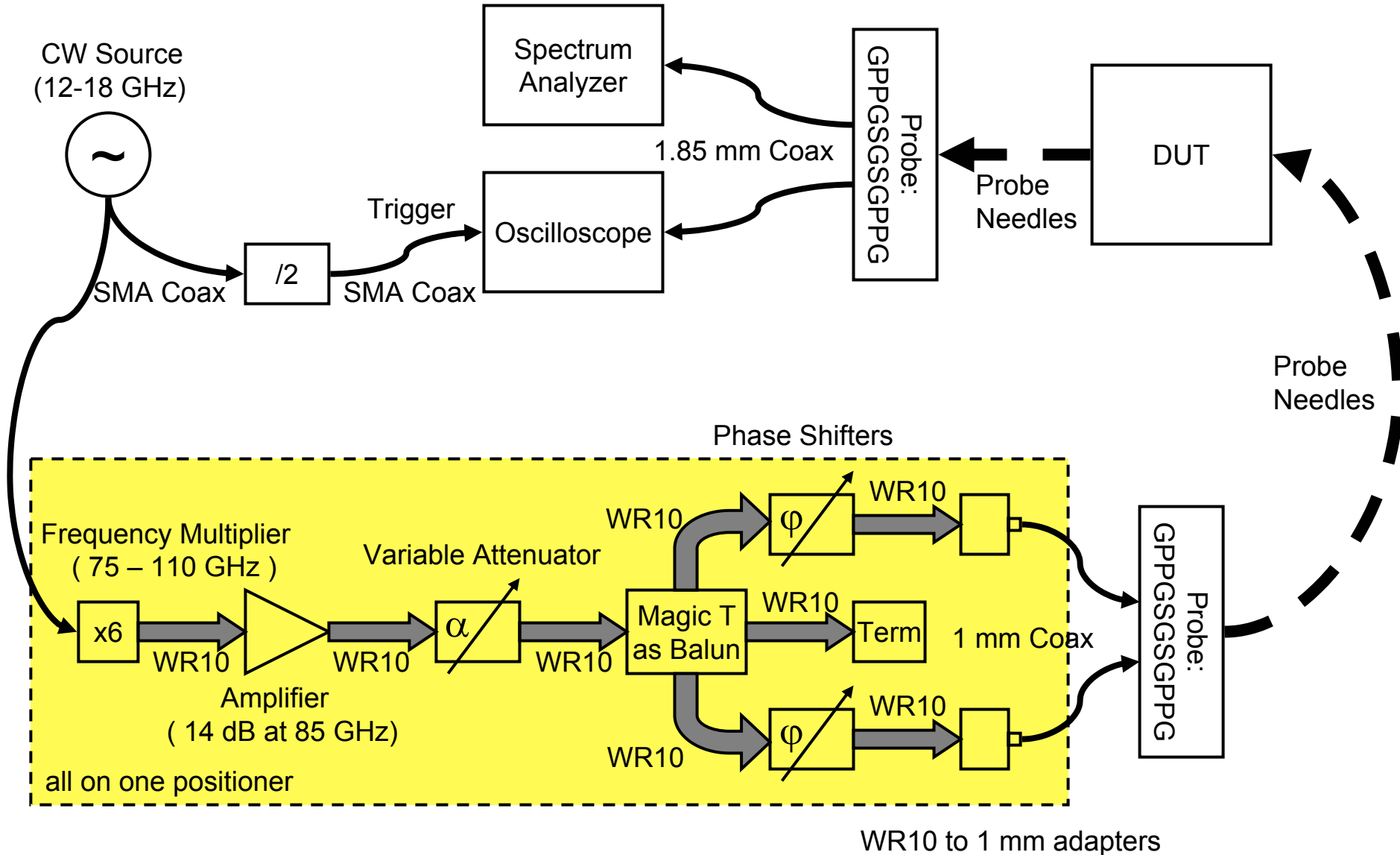
# Die Micrograph

CLOCK/2

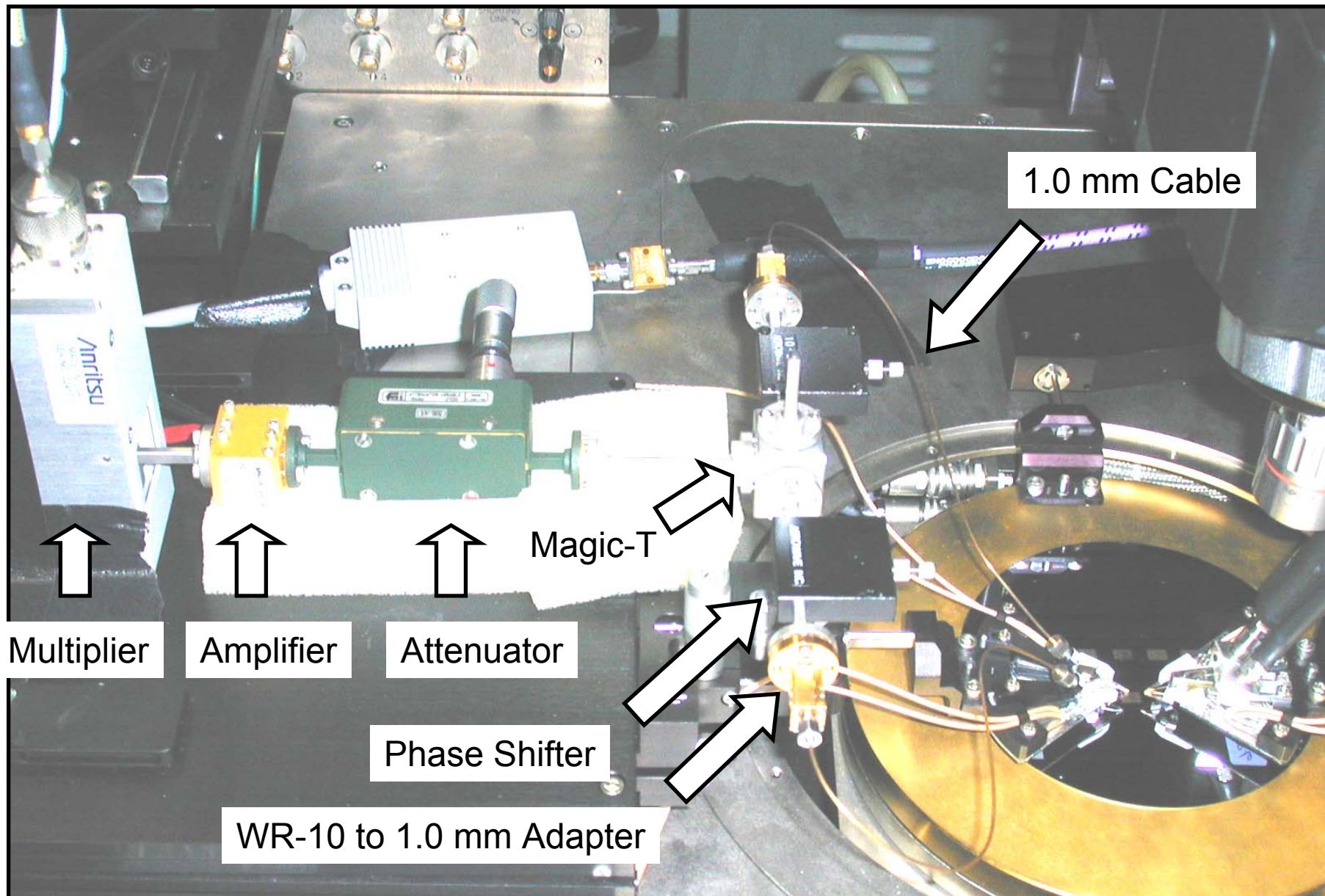


CLOCK

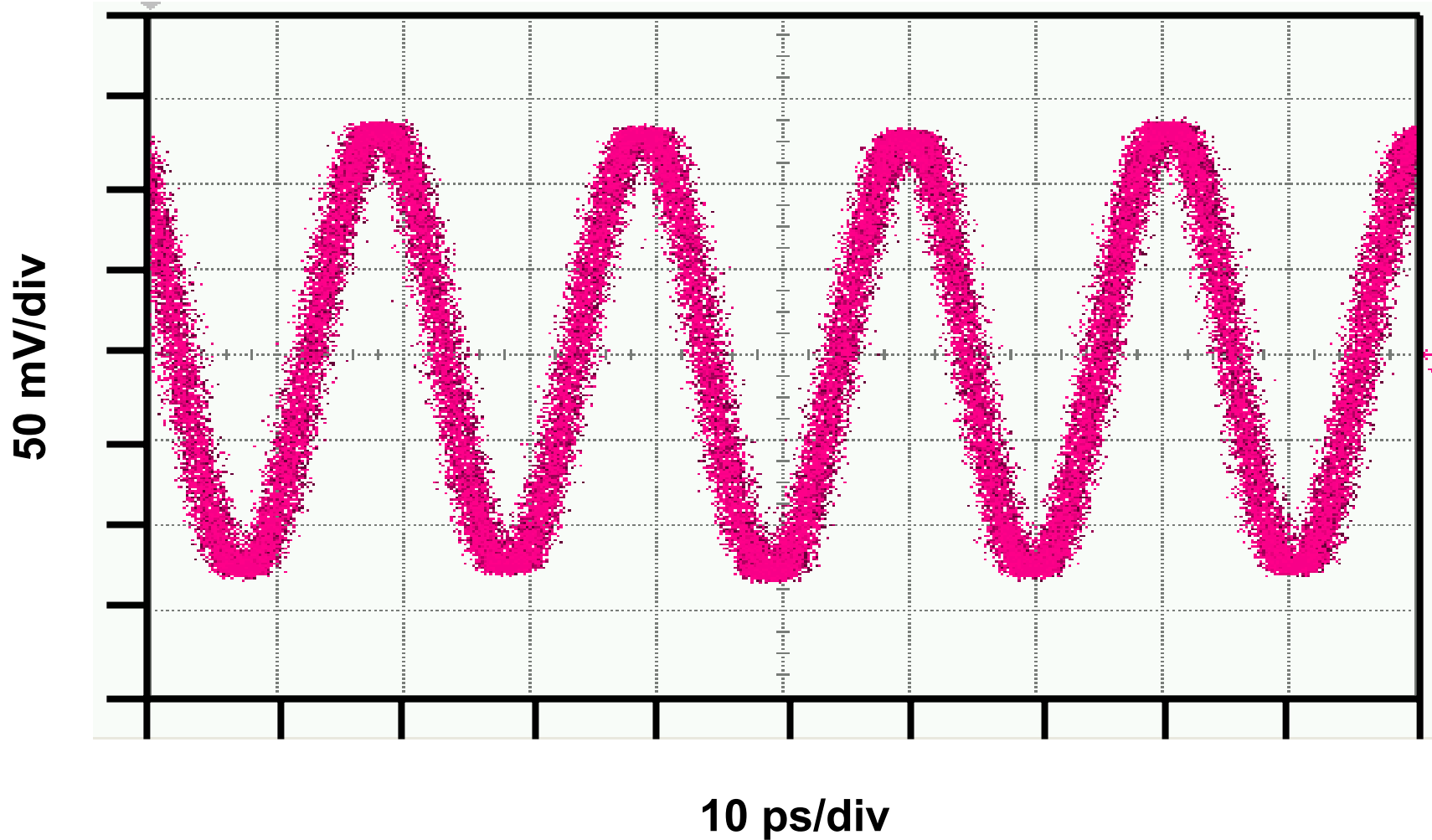
# Test Setup Block Diagram



# Test Setup



# 48.3 GHz Output Signal









# SiGe8HP and 7HP Frequency Dividers Performance Summary

	0.13 $\mu$ m SiGe (8HP)			0.18 $\mu$ m SiGe (7HP)		
	* Dynamic ECL	* Static ECL	† Static E <sup>2</sup> CL	* Static ECL	* Static ECLi	* Static E <sup>2</sup> CL
$V_{EE}$ (V)	-3.8	-3.8	-5.5	-3.6	-3.6	-5.2
$I_{EE}$ (mA)	75 <sup>1</sup>	68 <sup>1</sup>	140 <sup>1</sup>	32 <sup>2</sup>	80 <sup>1</sup>	66 <sup>2</sup>
$f_{SO}$ (GHz)	none	24	35	9	18	19
$f_{CLK}$ (GHz)	100	62	96	33	41	49

$f_{SO}$  is the frequency of self-oscillation

$f_{CLK}$  is the maximum input frequency

Dividers marked with '1': total current for the whole chip

Dividers marked with '2': estimate for divider core only

- Static ECL shows ~ 2x speed up (8HP vs 7HP, same design and power dissipation)
- Within same technology, E<sup>2</sup>CL is faster than plain ECL, but burns more power
- Inductive peaking (ECLi) also improves performance, trading off area

( \* Electronics Letters, Jan. 2003; † This work )

# Conclusion

A 96 GHz Static Frequency Divider was designed and tested in a 210 GHz  $f_T$  0.13  $\mu\text{m}$  SiGe bipolar technology

To our knowledge, this is the fastest static divider in any Si-based technology